



Bermuda Power Sequence

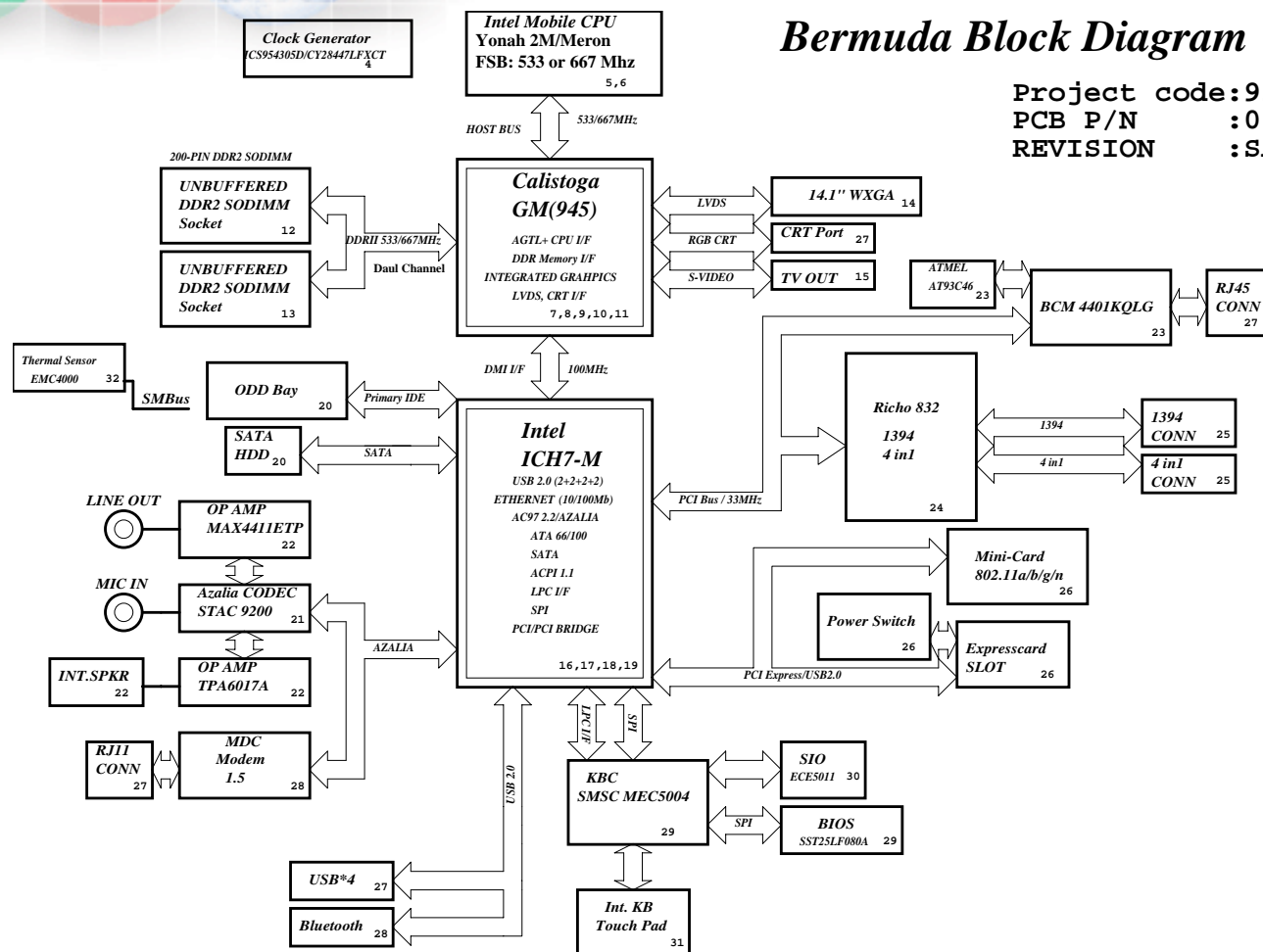


wistron



System DC/DC TP551120		39
INPUTS	OUTPUTS	
PWR_SRC	+5V5US +3V5US	
Battery Charger MAX8731		42
PWR_SRC	BATT+	
System DC/DC TPS51483		40
PWR_SRC	+1.05VRUN +1.5VRUN	
CPU DC/DC ADP3207 +ADP3419		38
PWR_SRC	VCC_CORE	
DDR2 DC/DC SC480		41
PWR_SRC	+1.8V5US +0.9VRUN +0.9V5US_DOR2VREF	

PCB LAYER
L1:TOP
L2:GND
L3:Signal
L4:Signal
L5:VCC
L6:Signal
L7:GND
L8:BOT







CPU_Core ADP3207+ADP3419

	Input signal	Output Signal	
RUNPWROK	EN	PWRGD	IMVP_PWRGD
VSSSENSE	FBRTN		
VCCSENSE	FB	CLKEN#	CLK_ENABLE#
DPRSLPVR	DPRSLP		
H_PSI#	PSI#		
H_DPRSTP#	DPRSTP#		
VID0~6	VID0~6		
	Input Power	Output Power	
+5V_RUN	VCC		+VCC_CORE



5V/3D3V TI TPS51120

	Input signal	Output Signal	
SUS_ON / THERM_STP#	EN1	VREG2	51120_VREF2
SUS_ON / THERM_STP#	EN2	VREG3	51120_3V
SUS_ON / THERM_STP#	EN3	VREG5	+5V_ALW
SUS_ON / THERM_STP#	EN5	PGOOD1	SUSPWROK_5V
GND	SKIPSEL	PGOOD2	SUSPWROK_5V
51120_VREF2	TONSEL		
5V_PWR	VO1		
3D3V_PWR	VO2		
	Input Power	Output Power	
<u>PWR_SRC_51120</u>	VIN		5V_PWR
			3D3V_PWR



1D5V/1D05V TI TP51483

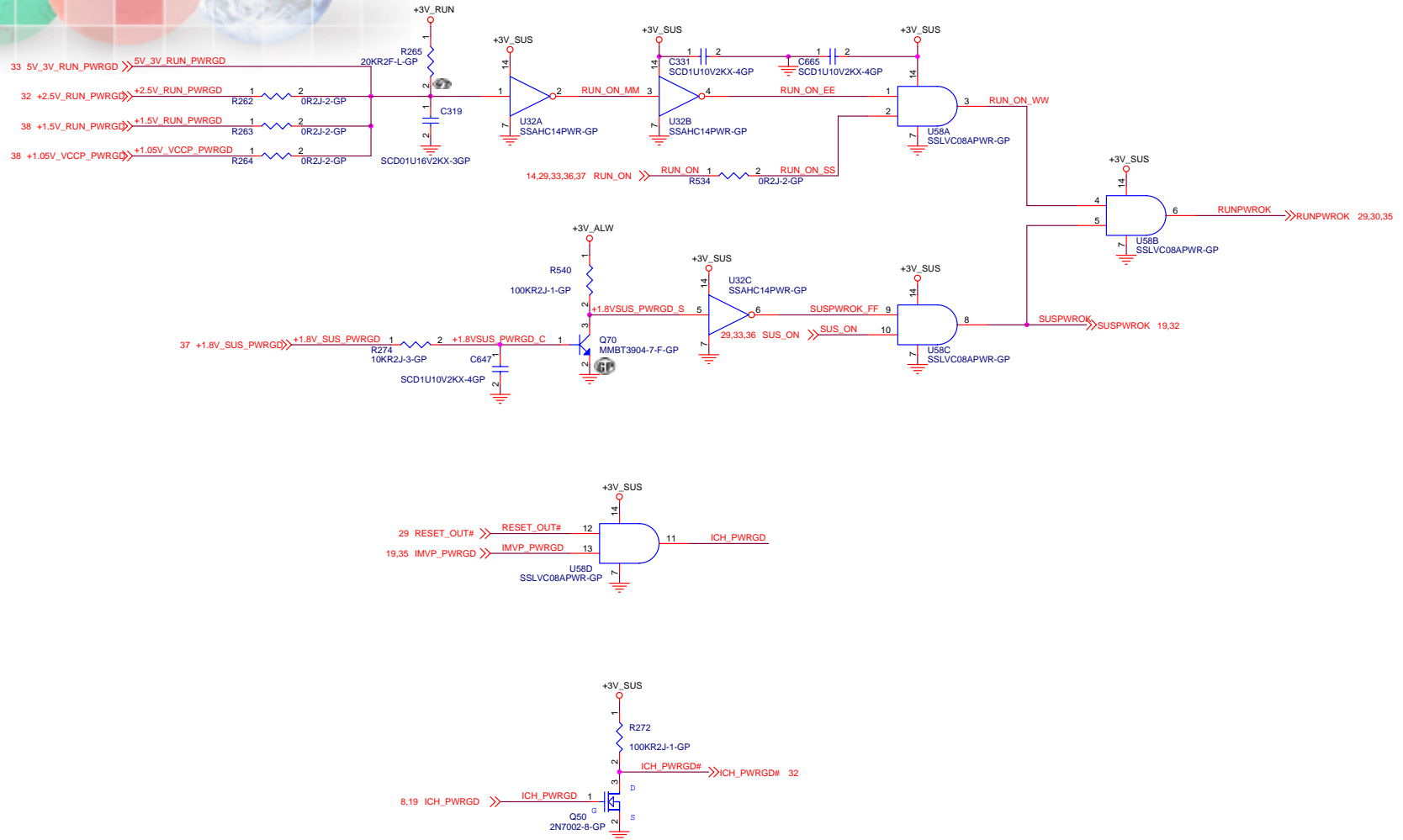
	Input signal	Output Signal	
RUN_ON_DC	EN/PSV2 (5V)	PGOOD2	+1.05V_VCCP_PWRGD
51483_TON2	TON2 (5V)		
RUN_ON_DC	EN/PSV1 (5V)	PGOOD1	+1.5V_RUN_PWRGD
51483_TON1	TON1 (5V)		
	Input Power	Output Power	
+1.05V_VCCP_P	VOUT2		
+5V_SUS	VCCA2		+1.5V_RUN_P
+5V_SUS	VDDP2		+1.05V_VCCP_P
+1.5V_RUN_P	VOUT1		
+5V_SUS	VCCA1		
+5V_SUS	VDDP1		

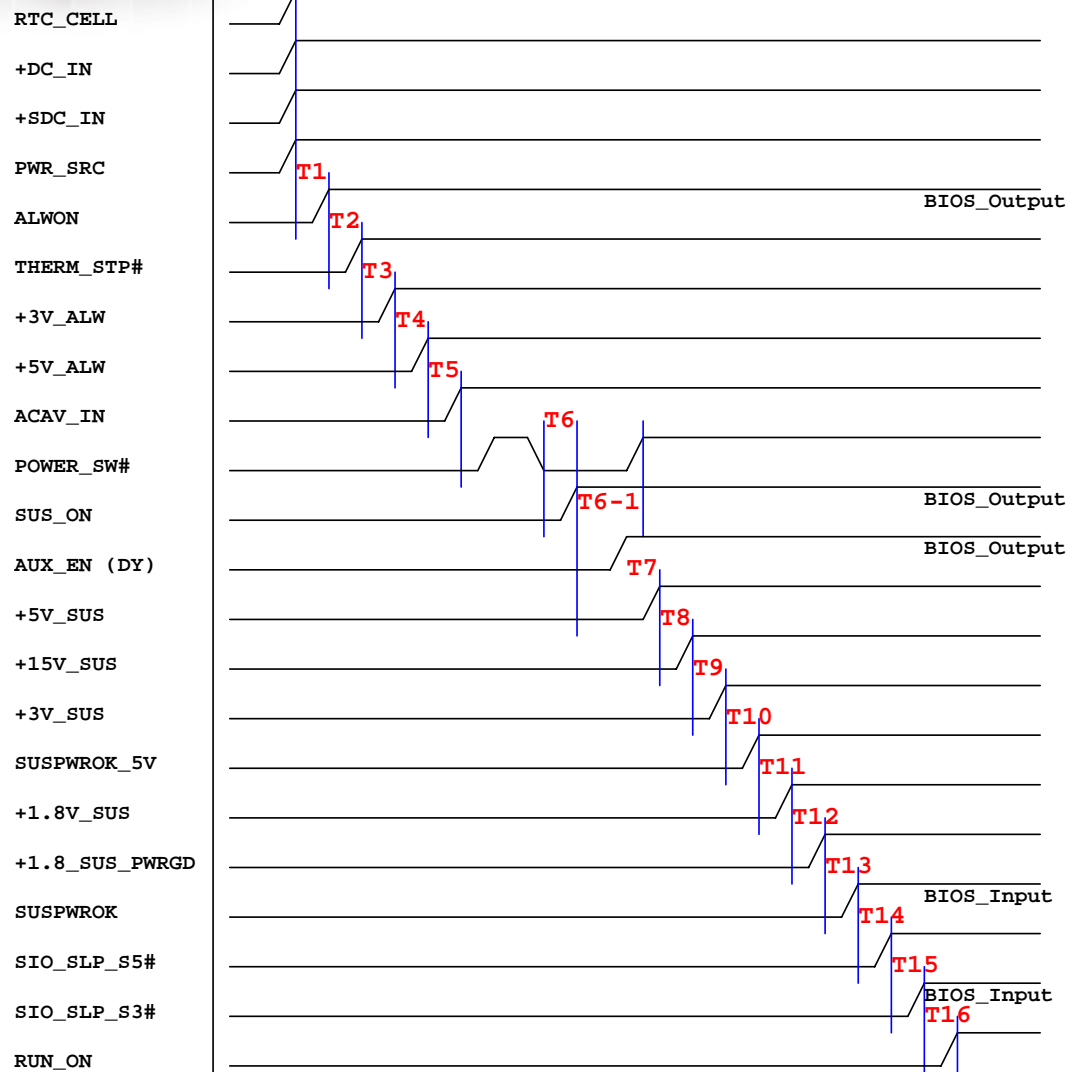


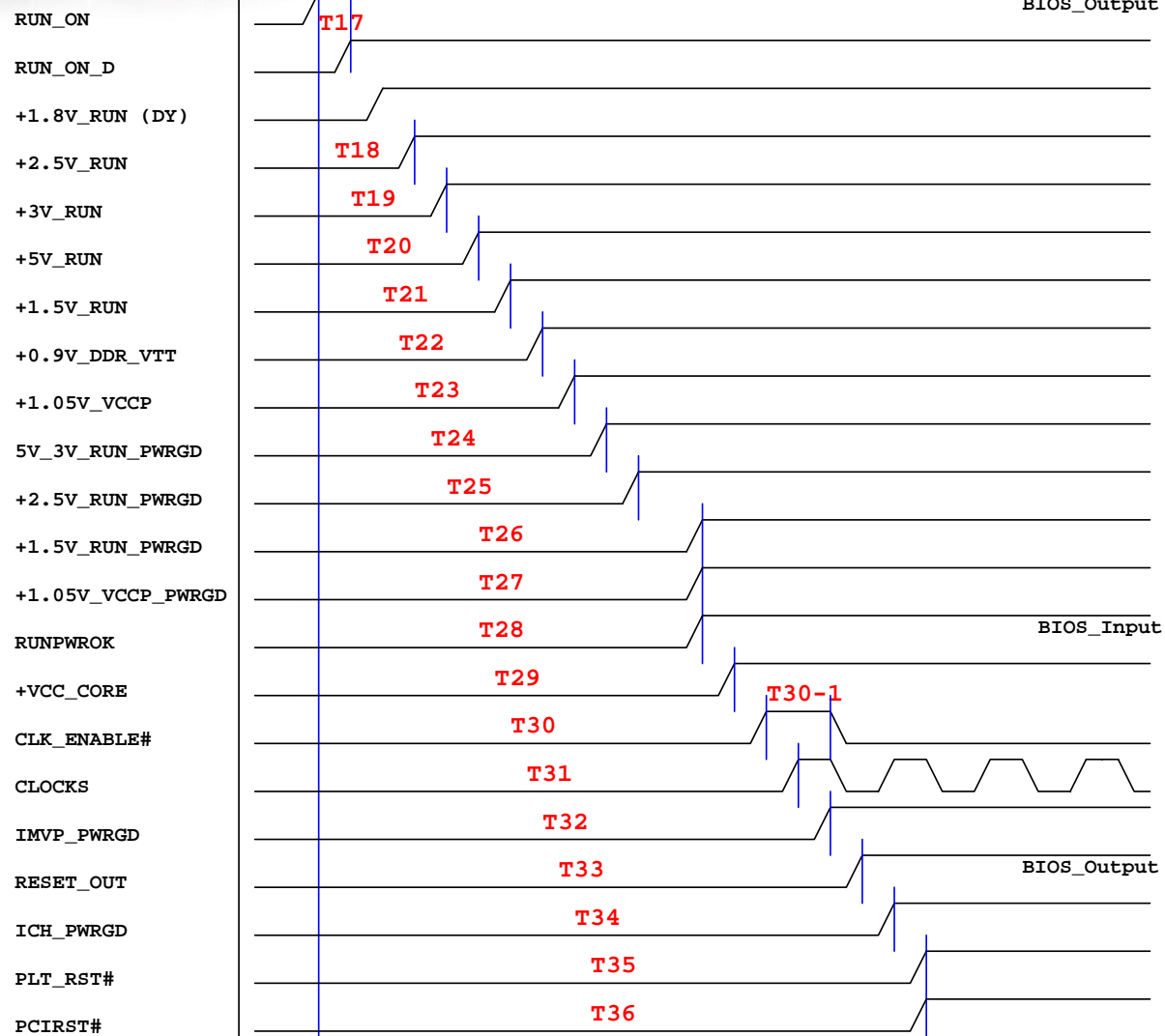
1D8V/0D9V TPS51116

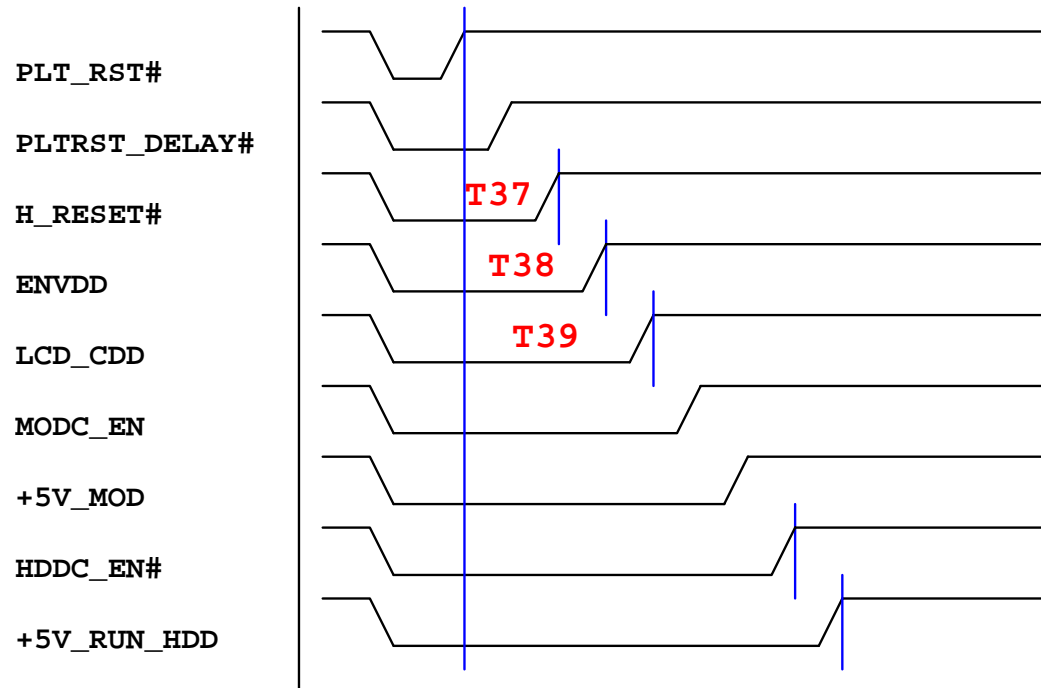
	Input signal	Output Signal	
SUSPWROK_5V	EN/PSV (5V)	PGD	+1.8V_SUS_PWRGD
RUN_ON	VTTEN (5V)		
1D8V_SUS_PWR	TON (<5V)		
+5V_SUS	VDDP (5V)		
	Input Power	Output Power	
1D8V_SUS_PWR	VTTIN	VTT	1D8V_SUS_PWR
+0.9V_DDR_VTTP	VTTS		+0.9V_DDR_VTTP
1D8V_SUS_PWR	VDDQS		
+5V_SUS	VCCA		













5.4 Power Sequencing

Pass[] Fail[] Testing[]

5.4.1 AC only

Pass[] Fail[] Testing[]

Test Purpose:	To record the timing sequence for the power rails.	
Overview of Procedure:	Measure the timing of the power rails. The definition of these timing variables is given in the power sequencing document attached below this table.	
Timing Variable	Time	Comments
T01	0mS	Time of PWR_SRC to ALWON
T02	7.4 uS	Time of ALWON to THERM_STP#
T03	920 uS	Time of THERM_STP# to +3V_ALW
T04	-568 uS	Time of +3V_ALW to +5V_ALW
T05	-286 uS	Time of +5V_ALW to ACAV_IN
T06	88 mS	Time of POWER_SW# to SUS_ON
T06-1	514 mS	fig8
T07	3.05 mS	Time of SUS_ON to +5V_SUS
T08	0 mS	Time of +5V_SUS to +15V_SUS
T09	0 mS	Time of +15V_SUS to +3V_SUS
T10	1.54mS	Time of +3V_SUS to SUSPWROK_5V
T11	200 uS	Time of SUSPWROK_5V to +1.8V_SUS
T12	2.52 mS	Time of +1.8V_SUS to +1.8V_SUS_PWRGD
T13	200 uS	Time of +1.8V_SUS_PWRGD to SUSPWROK
T14	98 mS	Time of SUSPWROK to SIO_SLP_S5#
T15	62uS	Time of SIO_SLP_S5# to SIO_SLP_S3#
T16	5.08uS	Time of SIO_SLP_S3# to RUN_ON
T17	5.24 mS	Time of RUN_ON to RUN_ON_D
T18	392 uS	Time of RUN_ON to +2.5V_RUN
T19	432 uS	Time of RUN_ON to +3V_RUN
T20	628 uS	Time of RUN_ON to +5V_RUN
T21	1.18 mS	Time of RUN_ON to +1.5V_RUN
T22	5.04 mS	Time of RUN_ON to +0.9V_DDR_VTT
T23	1.26 mS	Time of RUN_ON to +1.05V_VCCP
T24	2.78 mS	Time of RUN_ON to 5V_3V_RUN_PWRGD
T25	2.88 mS	Time of RUN_ON to +2.5V_RUN_PWRGD
T26	1.18 mS	Time of RUN_ON to +1.5V_RUN_PWRGD
T27	2.88 mS	Time of RUN_ON to +1.05V_RUN_PWRGD
T28	2.24 mS	Time of RUN_ON to RUNPWROK
T29	3.86 mS	Time of RUN_ON to +VCC_CORE
T30	432uS	Time of RUN_ON to CLK_ENABLE#
T30-1	4.14 mS	fig33
T31	406 uS	Time of RUN_ON to CLOCKS
T32	11.8 mS	Time of RUN_ON to IMVP_PWRGD
T33	328 mS	Time of RUN_ON to RESET_OUT
T34	324 mS	Time of RUN_ON to ICH_PWRGD
T35	324 mS	Time of RUN_ON to PLT_RST#
T36	328 mS	Time of RUN_ON to PCIRST#



DB2 Board Bring-Up Document

T37	1.01 mS	Time of PLT_RST# to H_RESET#
T38	2.78 S	Time of PLT_RST# to ENVDD
T39	4.64 S	Time of PLT_RST# to LCD_CDD
Section Owner:	Peace Yin	
Section Tester:	Shihwoei Sun , Doop Sun	
Time To Complete:		
Date Finished:		

Fig. 1 Time of +DC_IN to +SDC_IN

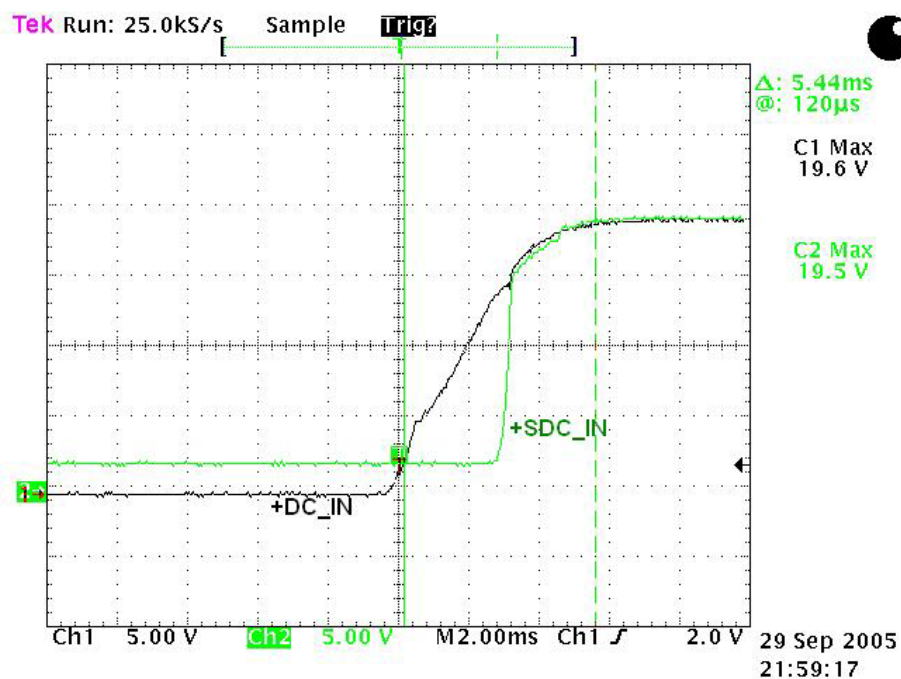


Fig. 2 Time of PWR_SRC to ALWON

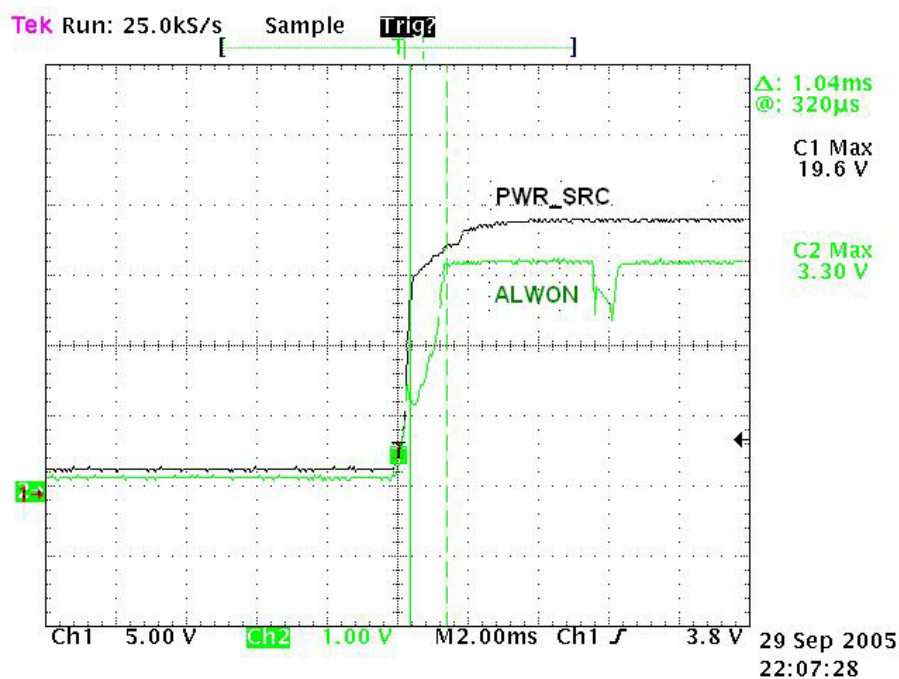


Fig. 3 Time of ALWON to THERM_STP#

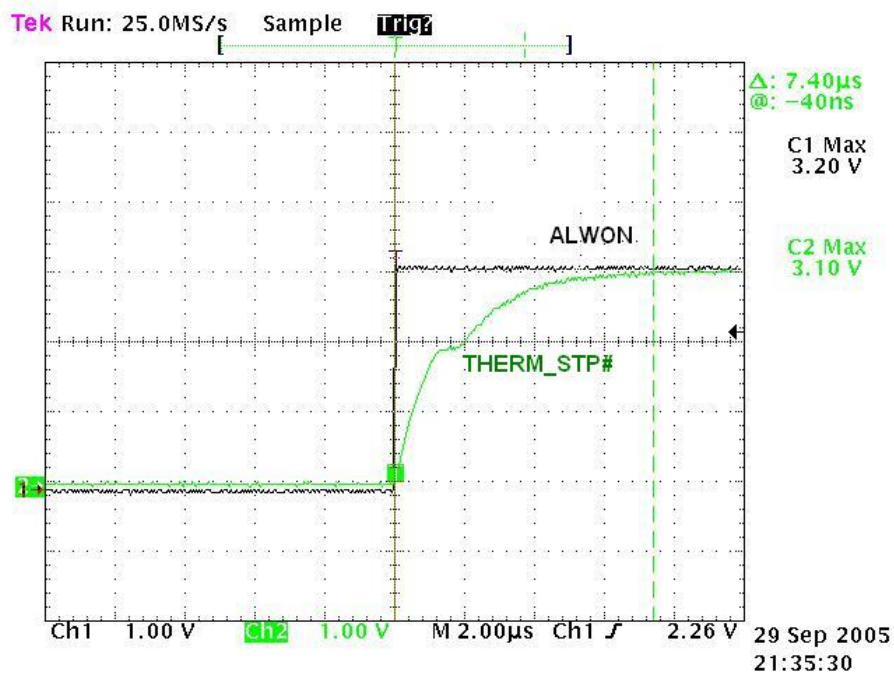


Fig. 4 Time of THERM_STP# to +3V_ALW

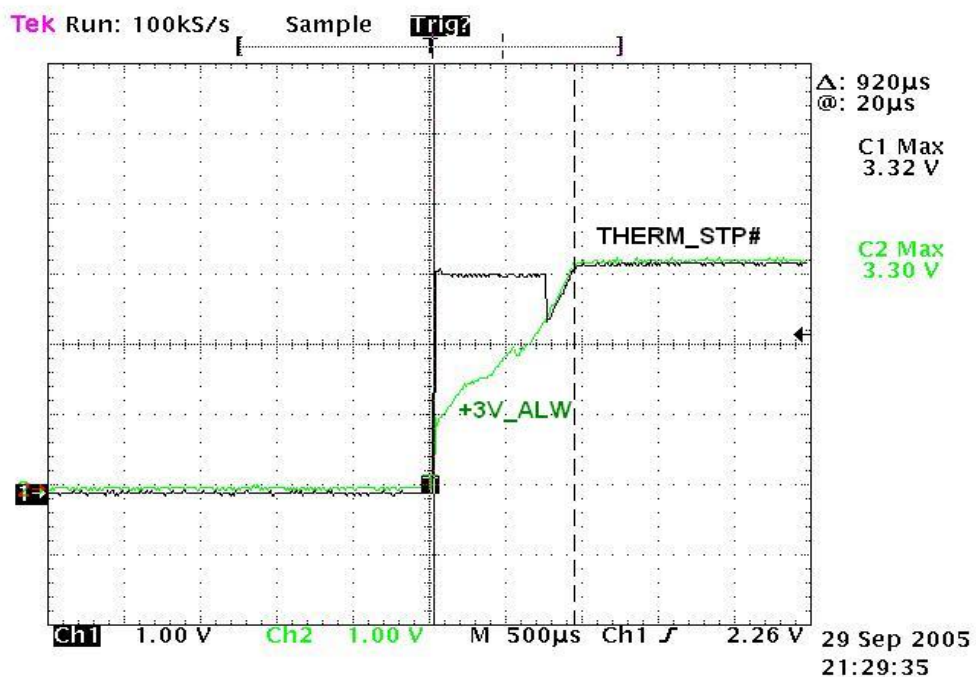




Fig. 5 Time of +3V_ALW to +5V_ALW

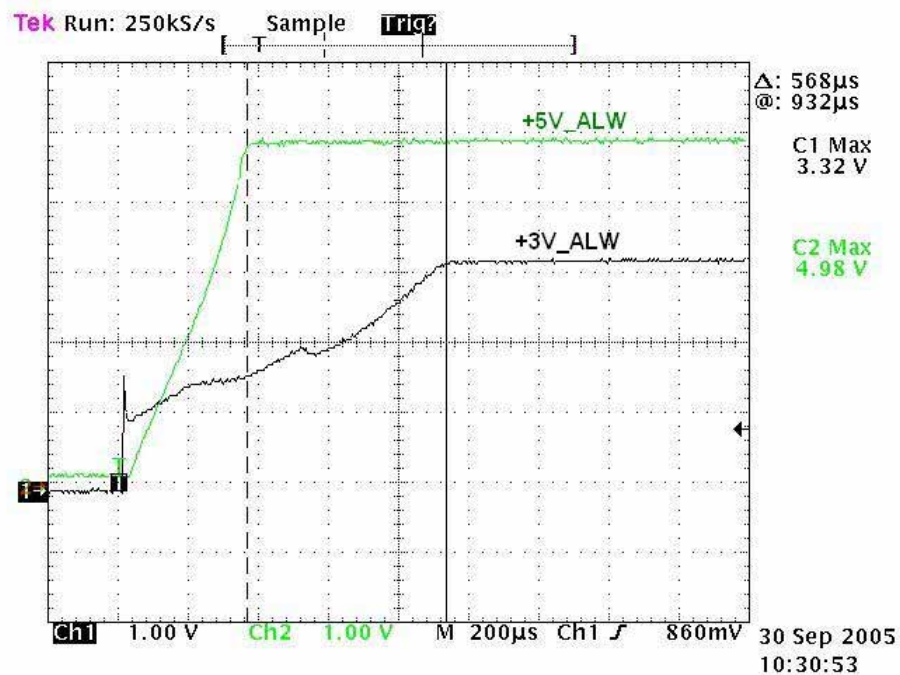


Fig. 6 Time of +5V_ALW to ACAV_IN

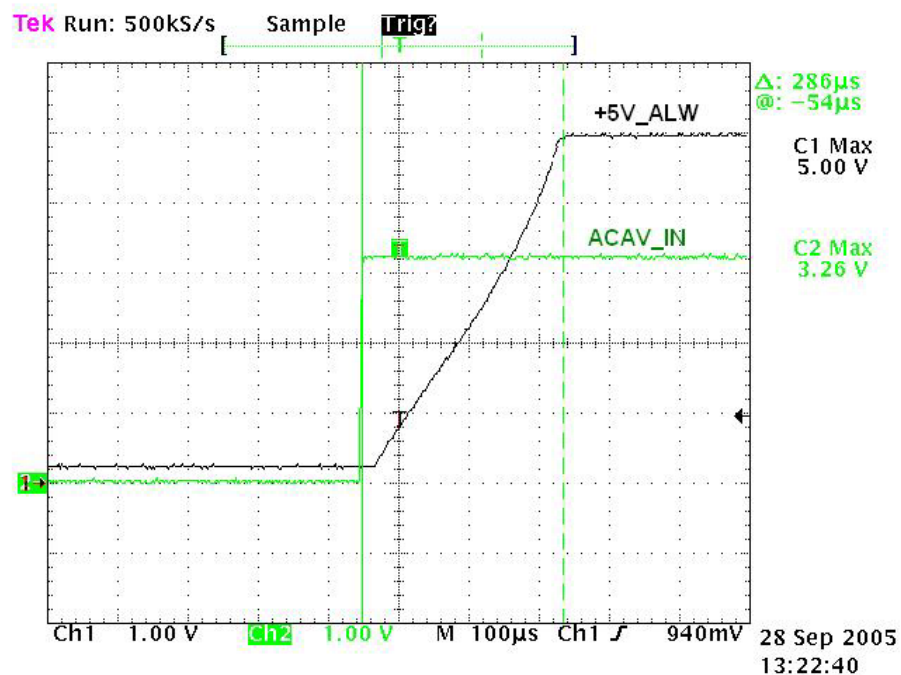


Fig.7 Time of POWER_SW# to SUS_ON-A

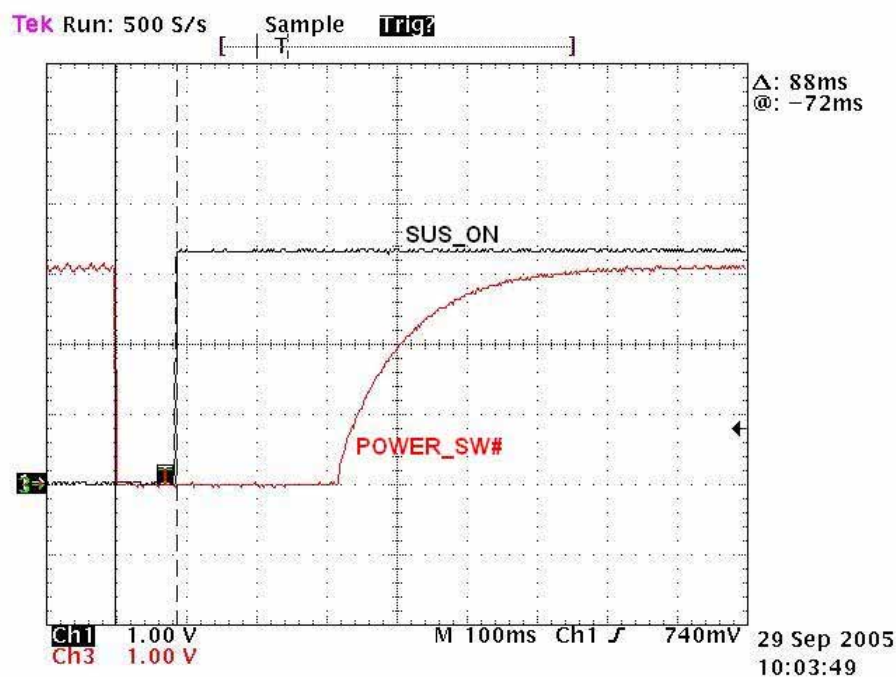


Fig.8 Time of POWER_SW# to SUS_ON-B

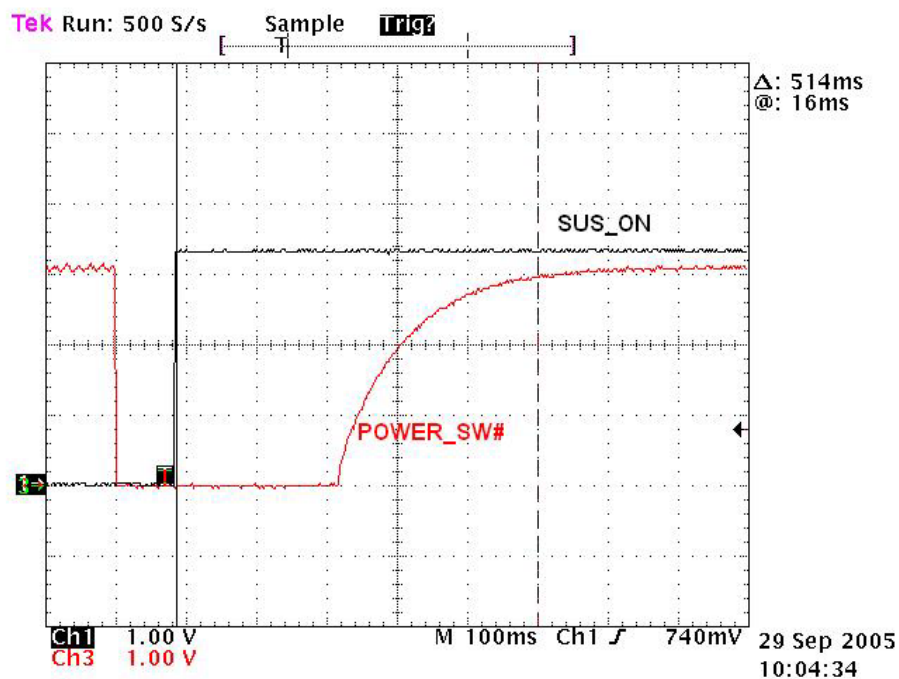


Fig.9 Time of SUS_ON to +5V_SUS

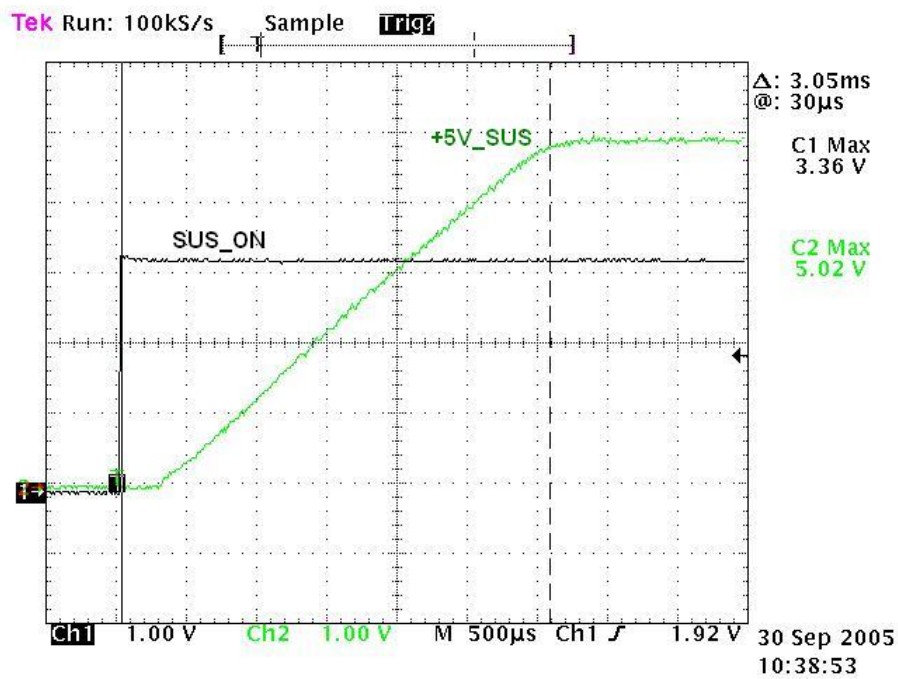


Fig.10 Time of +5V_SUS to +15V_SUS

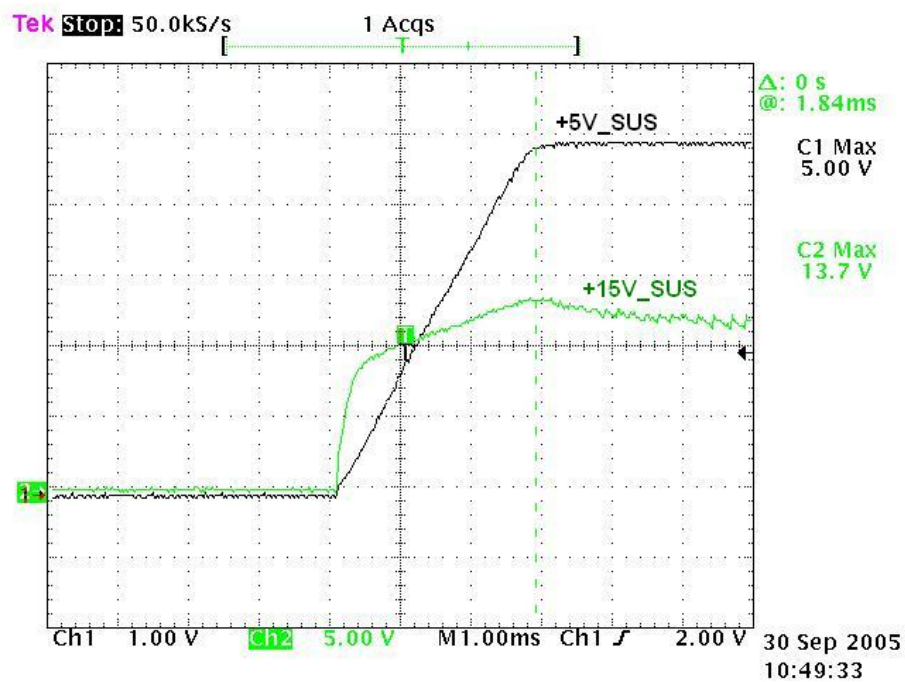


Fig.11 Time of +15V_SUS to +3V_SUS

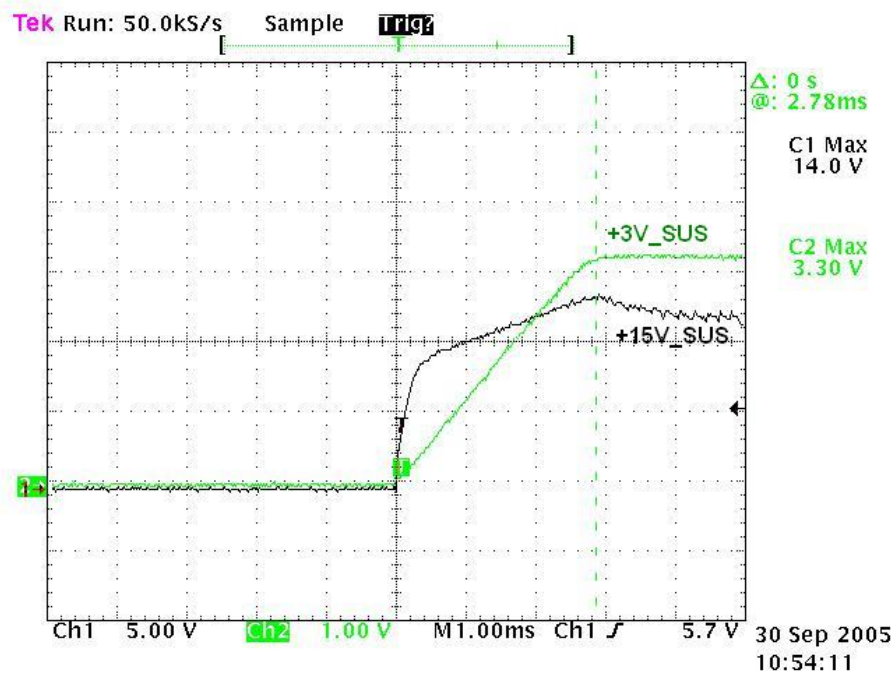


Fig.12 Time of +3V_SUS to SUSPWROK_5V

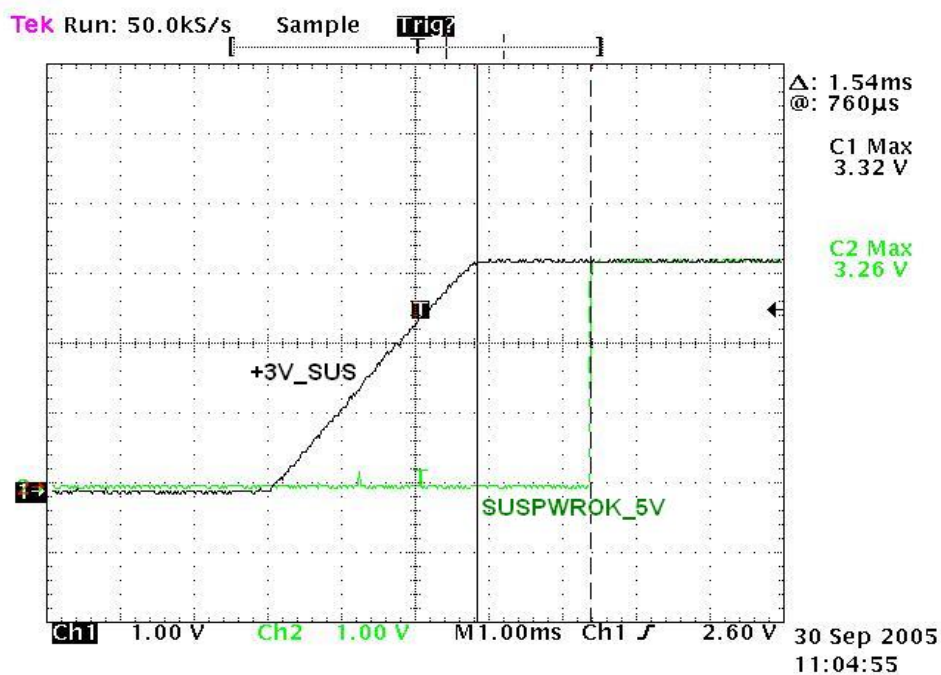




Fig.13 Time of SUSPWROK_5V to +1.8V_SUS

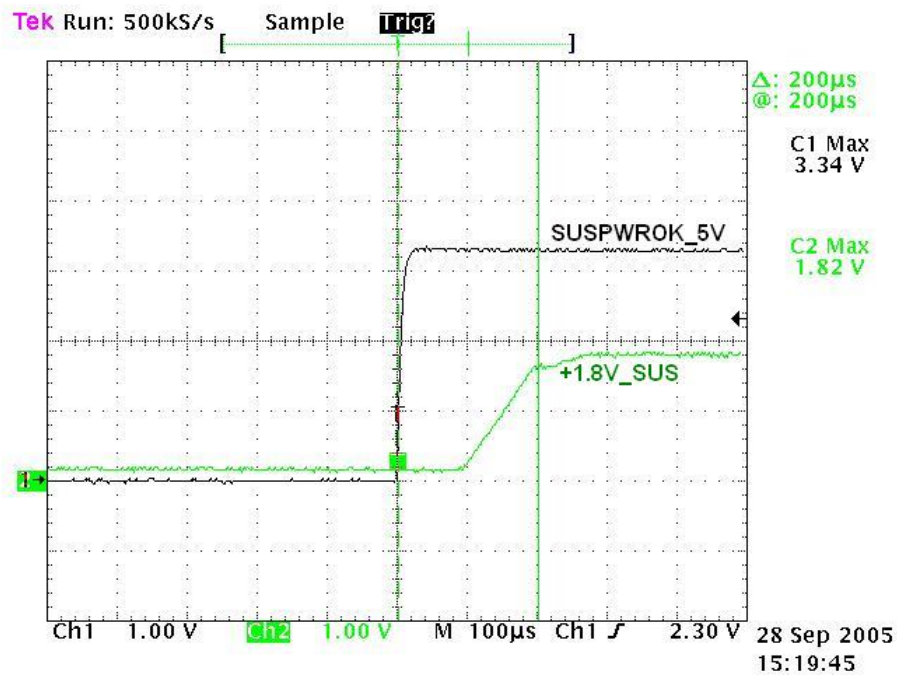


Fig.14 Time of +1.8V_SUS to +1.8V_SUS_PWRGD

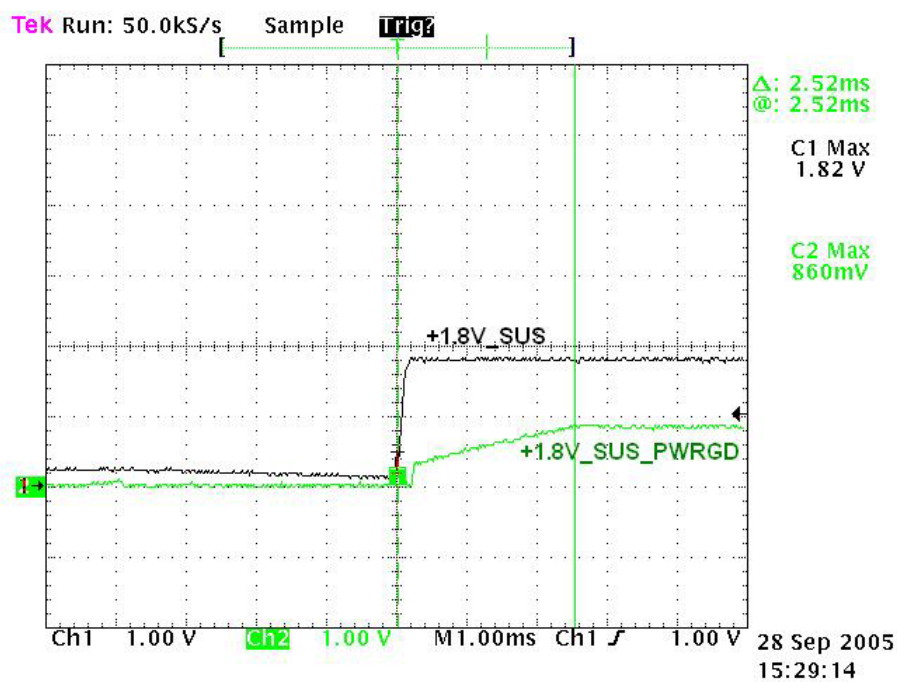


Fig.15 Time of +1.8V_SUS_PWRGD to SUSPWROK

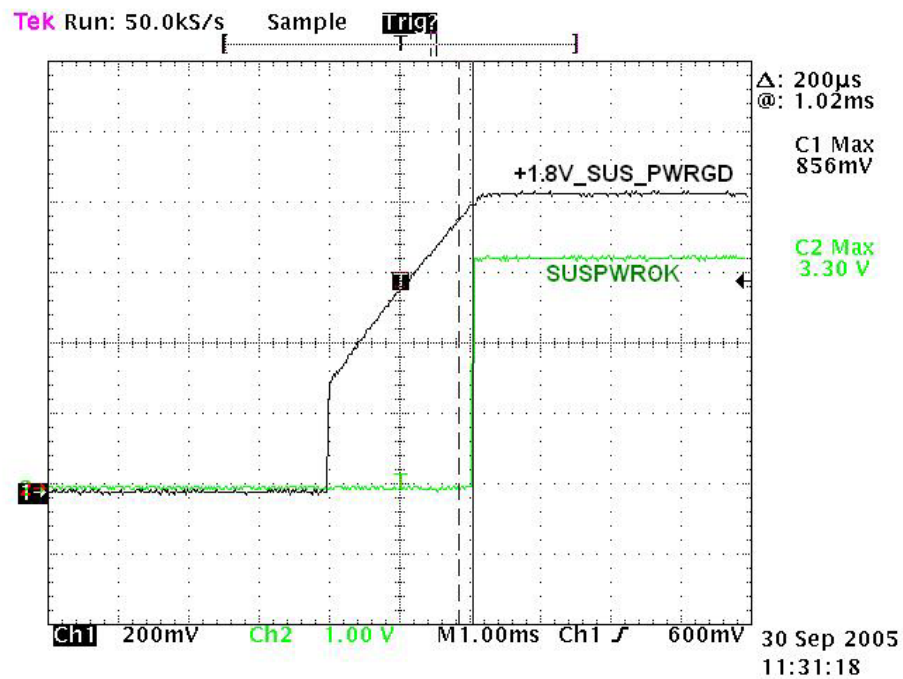


Fig.16 Time of SUSPWROK to SIO_SLP_S5#

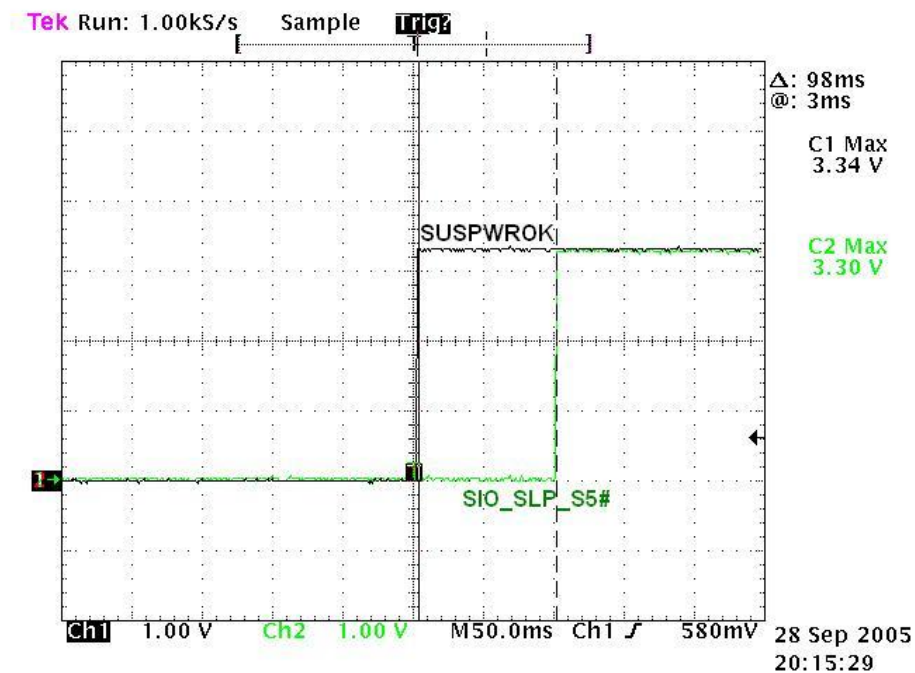




Fig.17 Time of SIO_SLP_S5# to SIO_SLP_S3#

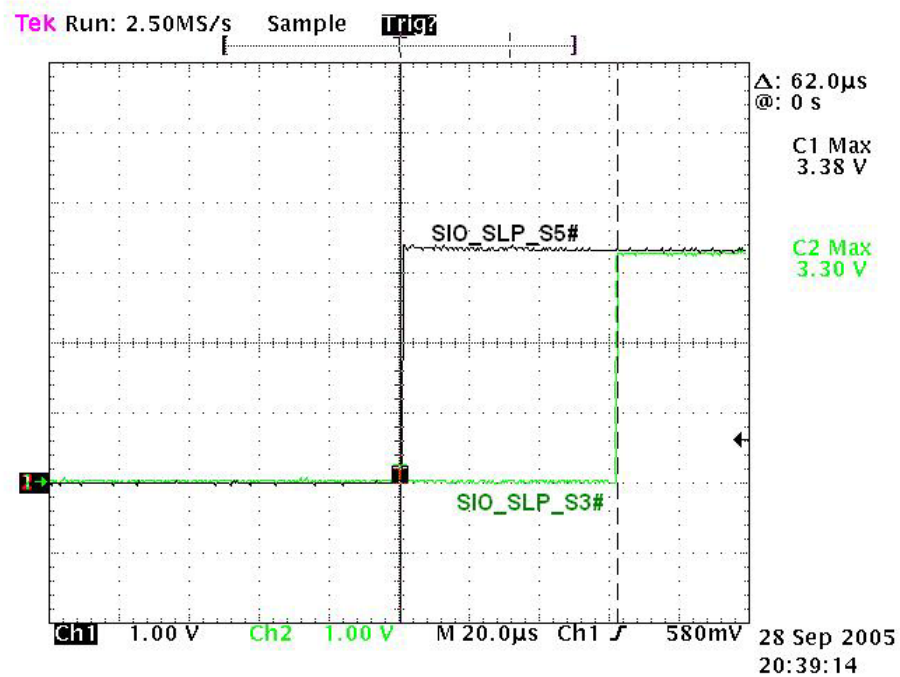


Fig.18 Time of SIO_SLP_S3# to RUN_ON

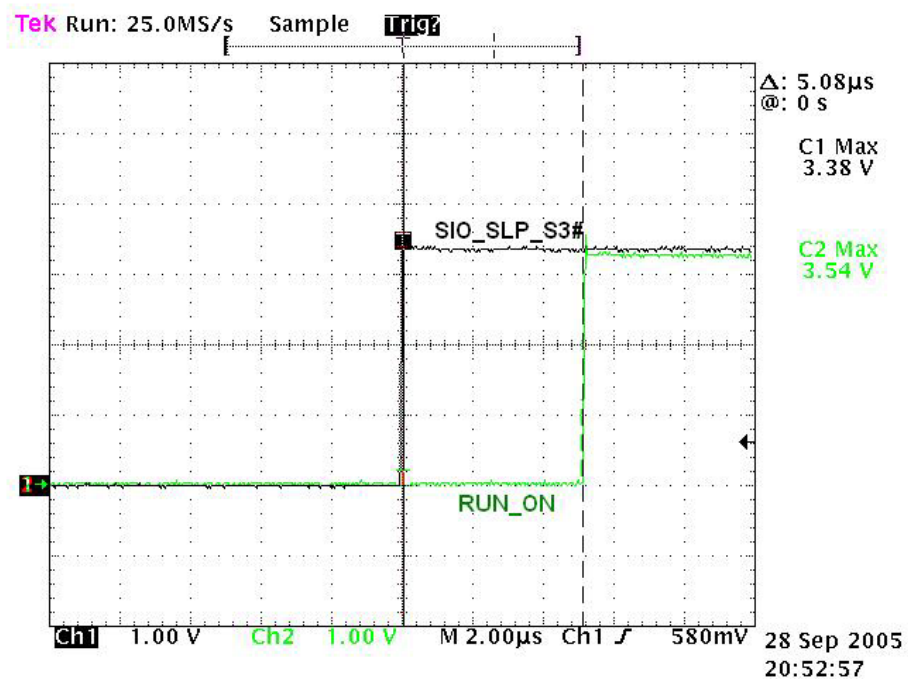


Fig.19 Time of RUN_ON to RUN_ON_D

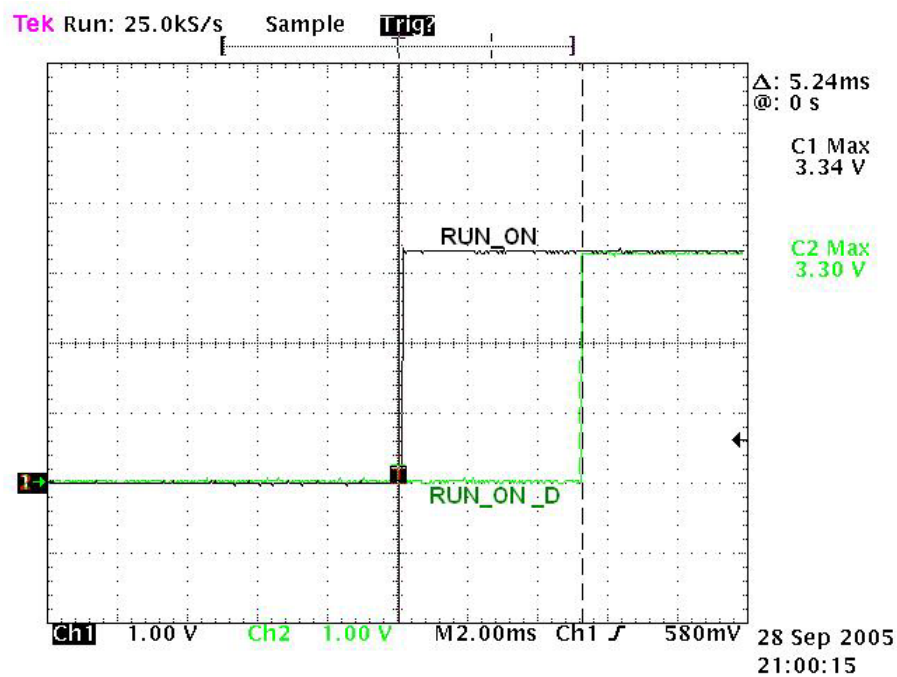


Fig.20 Time of RUN_ON to +2.5V_RUN

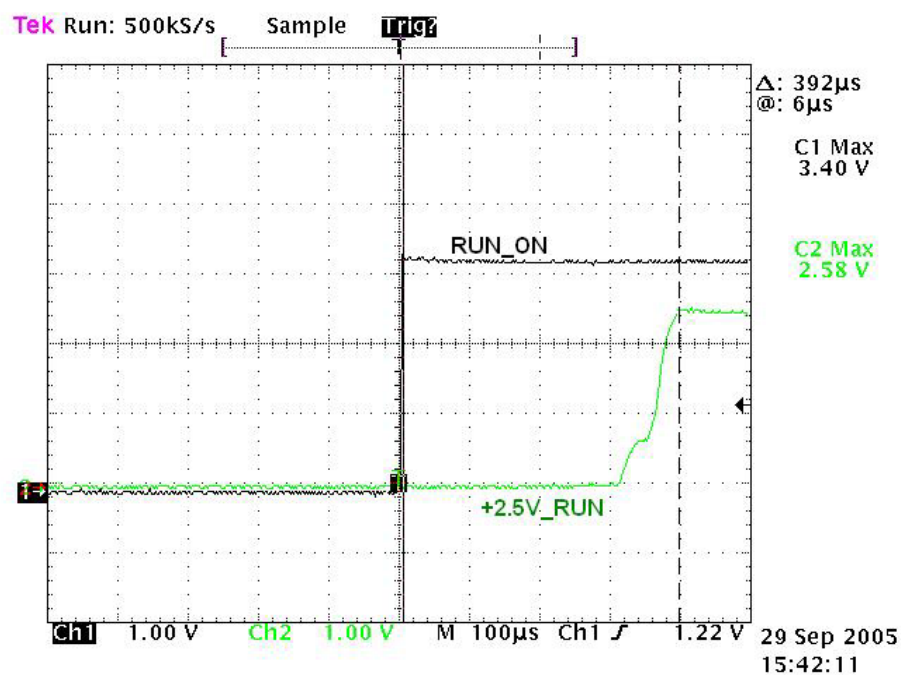


Fig.21 Time of RUN_ON to +3V_RUN

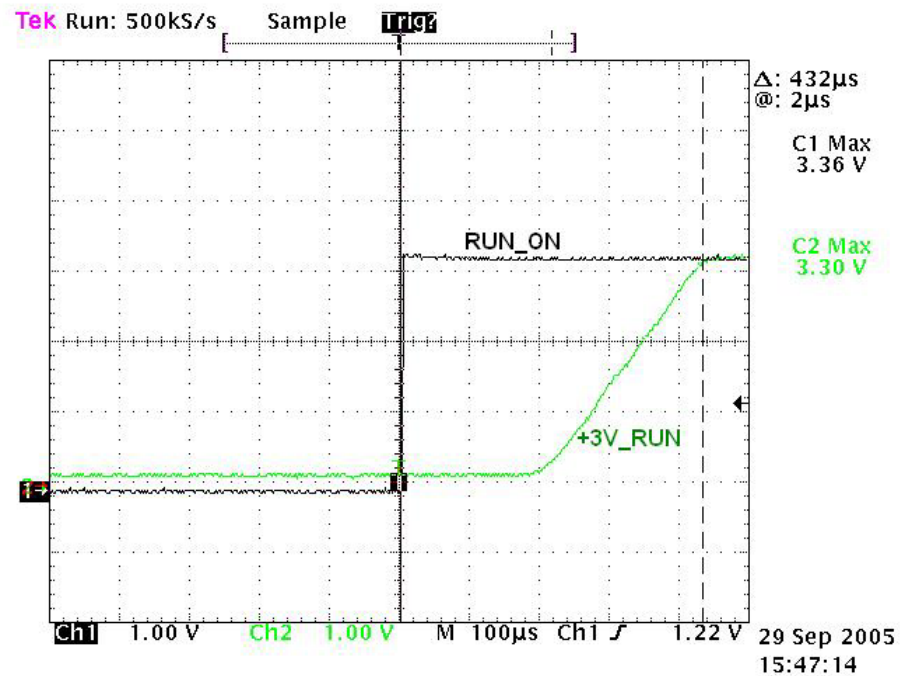


Fig.22 Time of RUN_ON to +5V_RUN

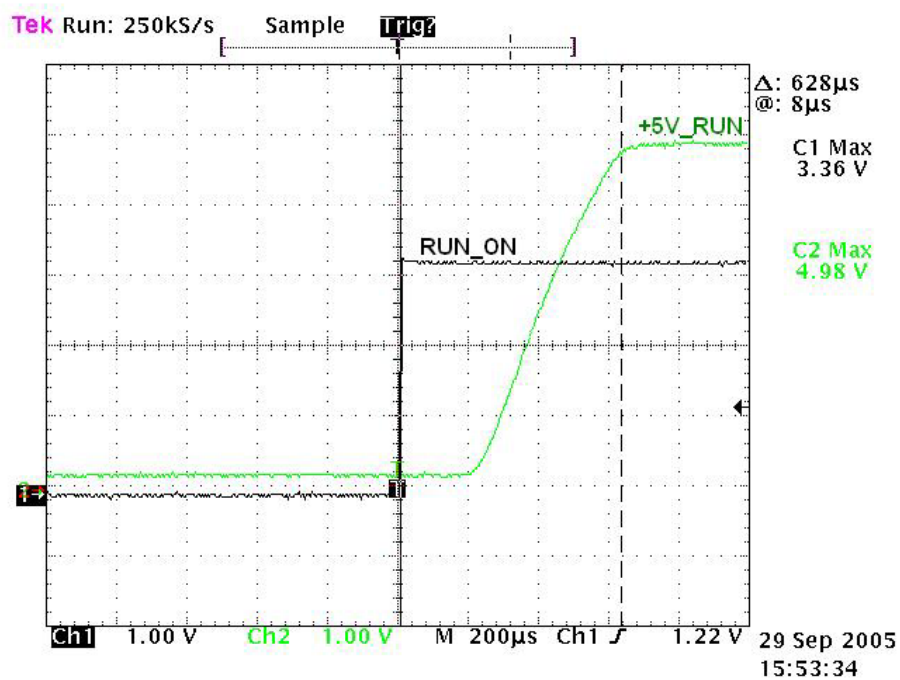


Fig.23 Time of RUN_ON to +1.5V_RUN

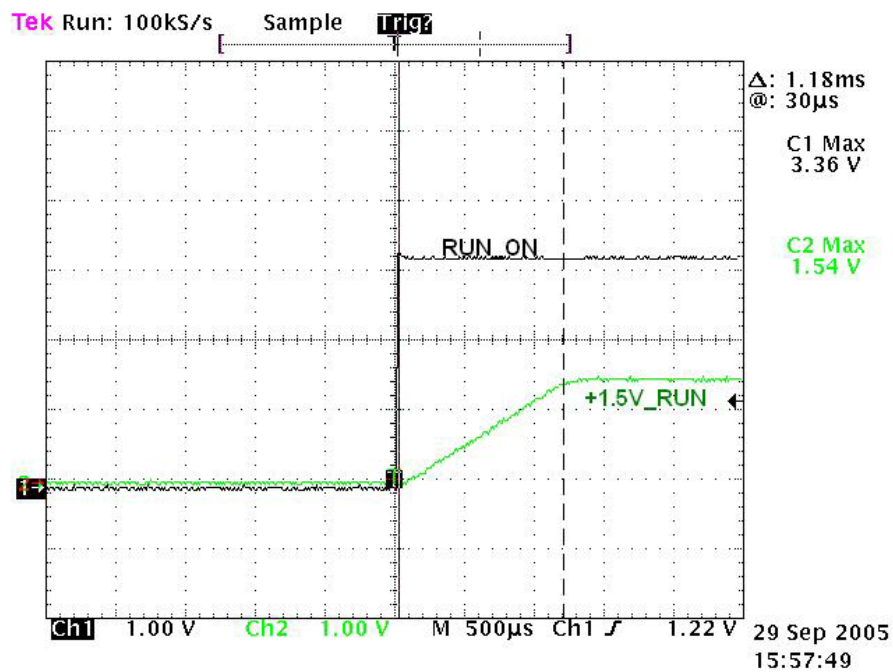


Fig.24 Time of RUN_ON to +0.9V_DDR_VTT

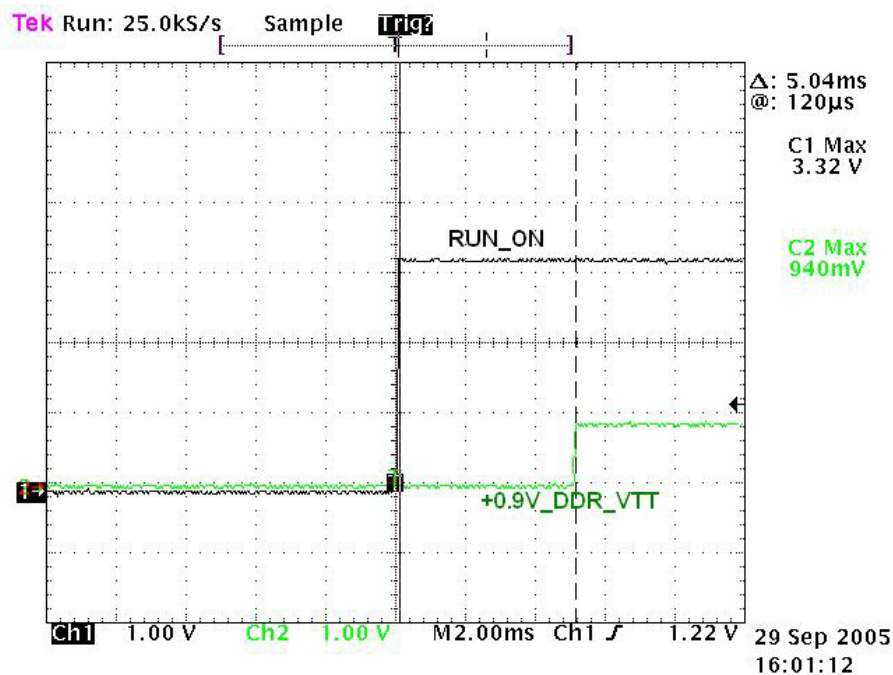




Fig.25 Time of RUN_ON to +1.05V_VCCP

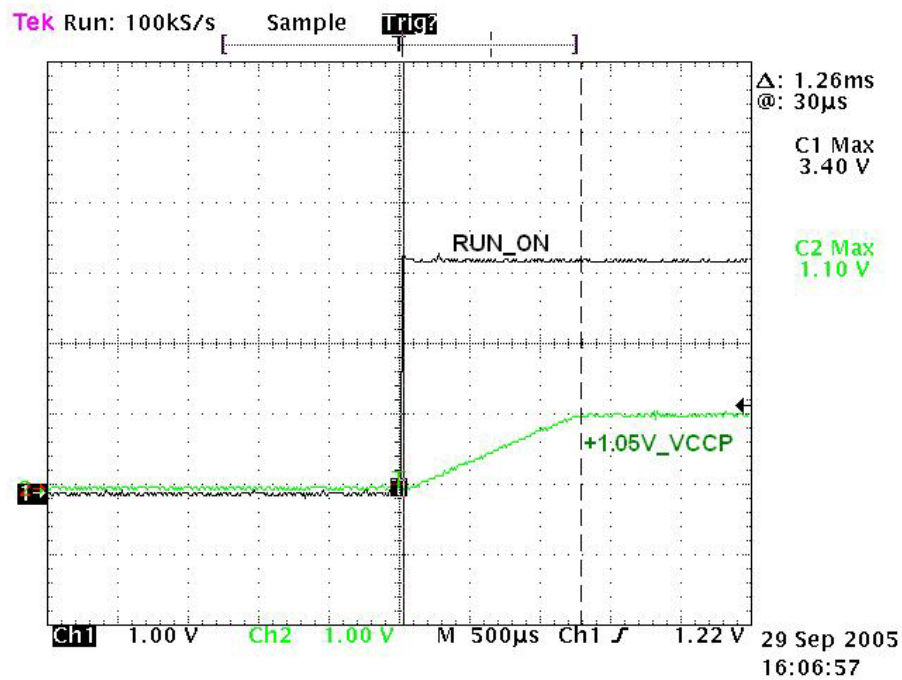


Fig.26 Time of RUN_ON to 5V_3V_RUN_PWRGD

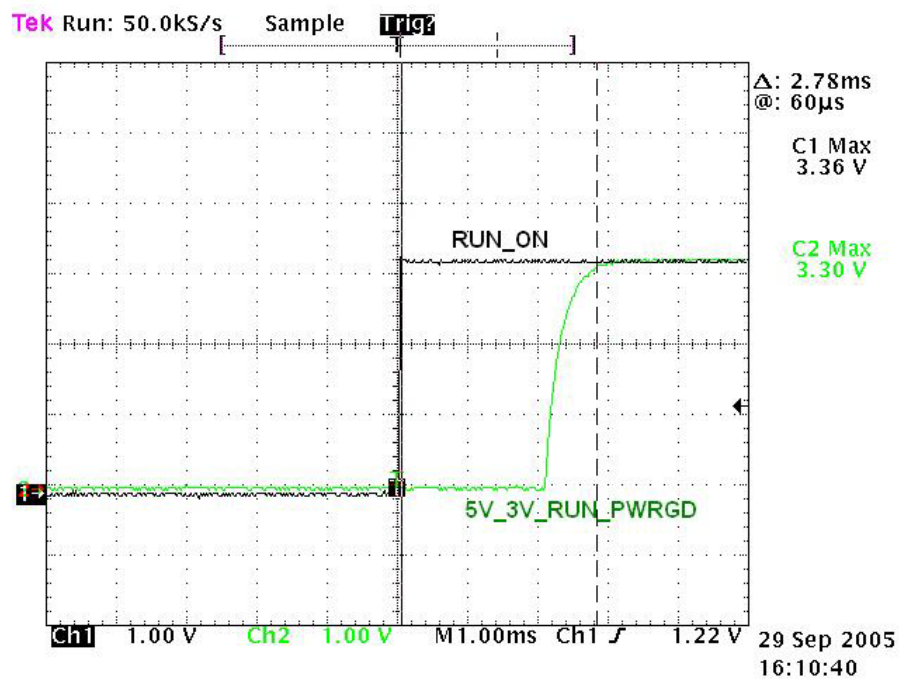




Fig.27 Time of RUN_ON to +2.5V_RUN_PWRGD

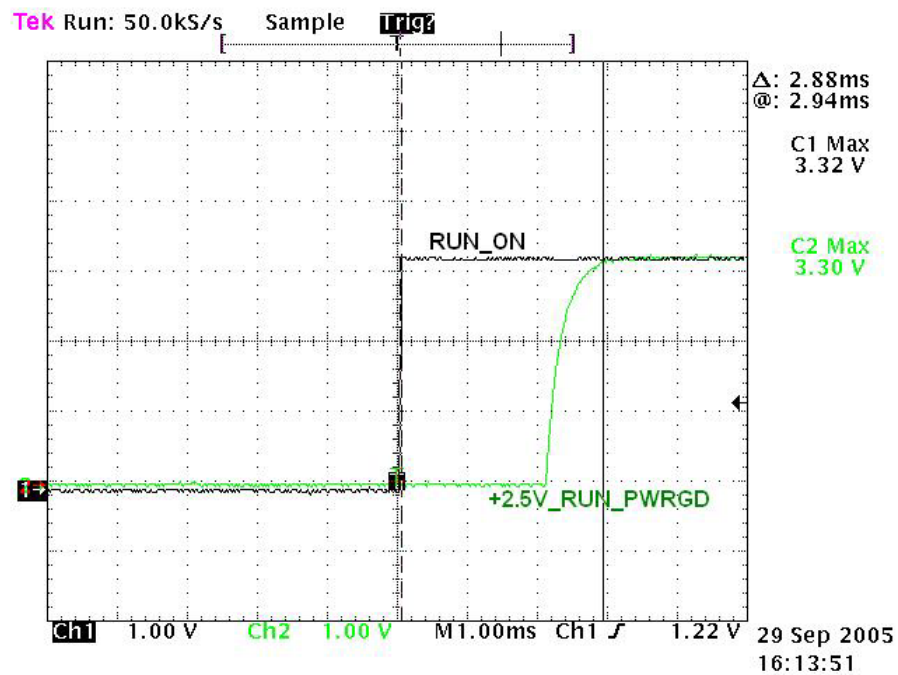


Fig.28 Time of RUN_ON to +1.5V_RUN_PWRGD

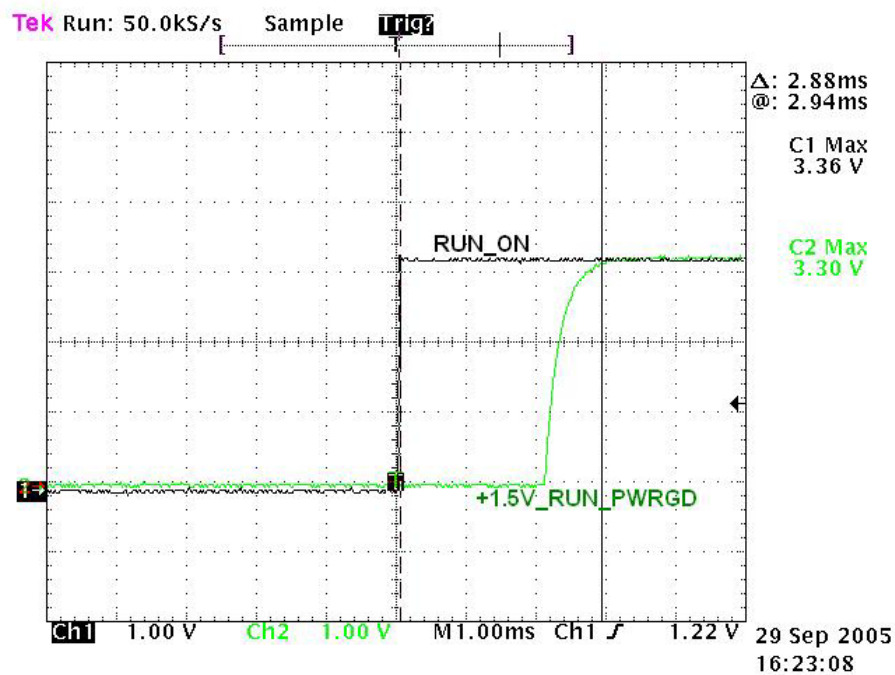


Fig.29 Time of RUN_ON to +1.05V_VCCP_PWRGD

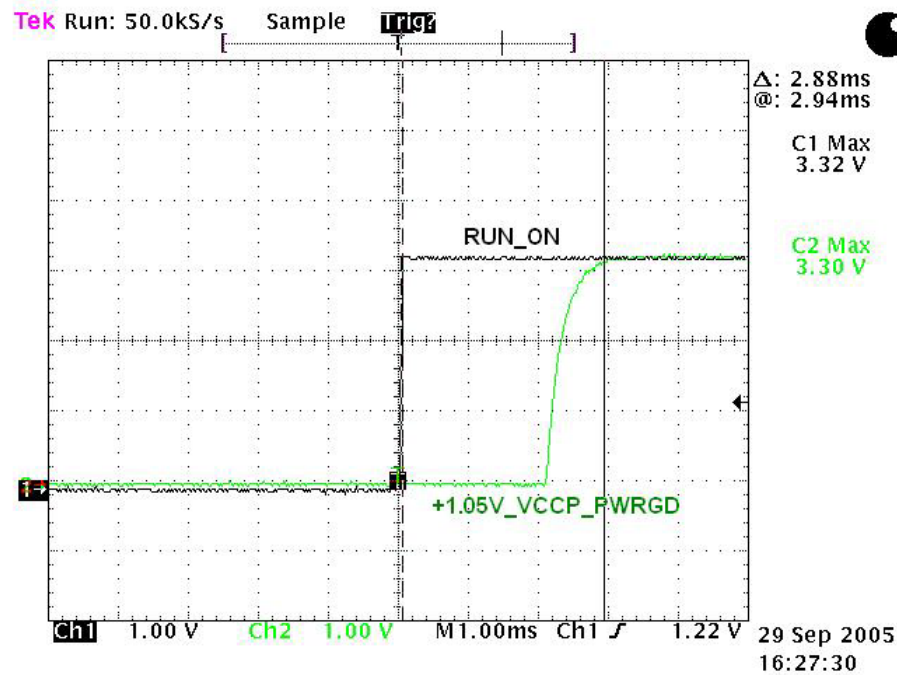


Fig.30 Time of RUN_ON to RUNPWROK

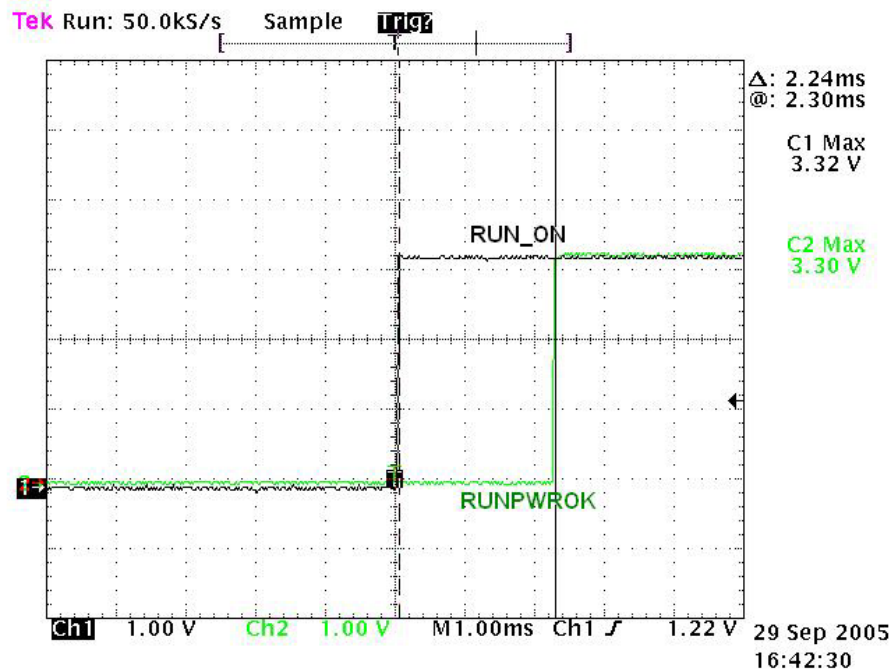


Fig.31 Time of RUN_ON to +VCC_CORE

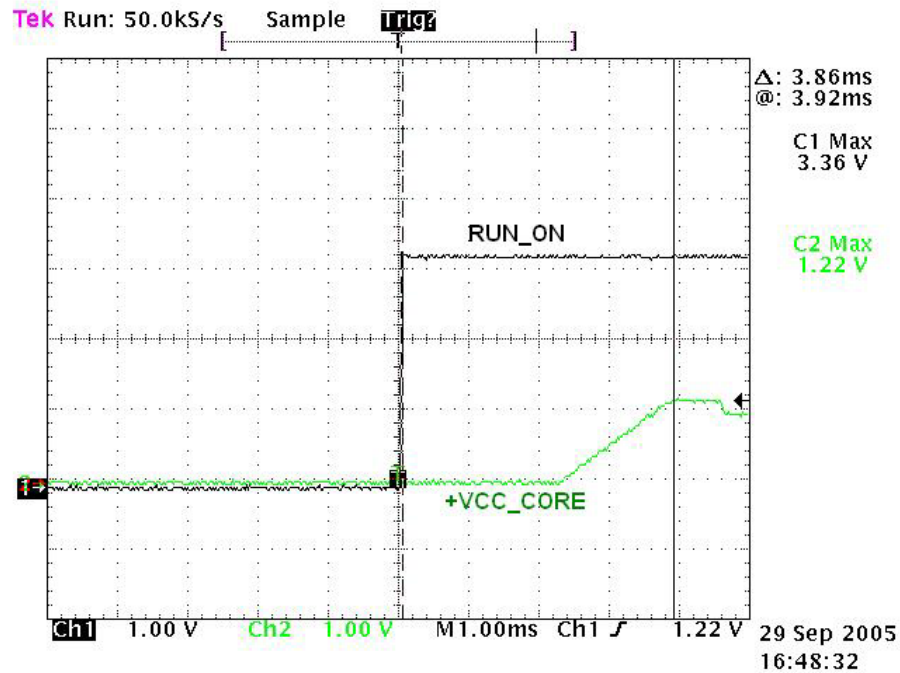


Fig.32 Time of RUN_ON to CLK_ENABLE# -A

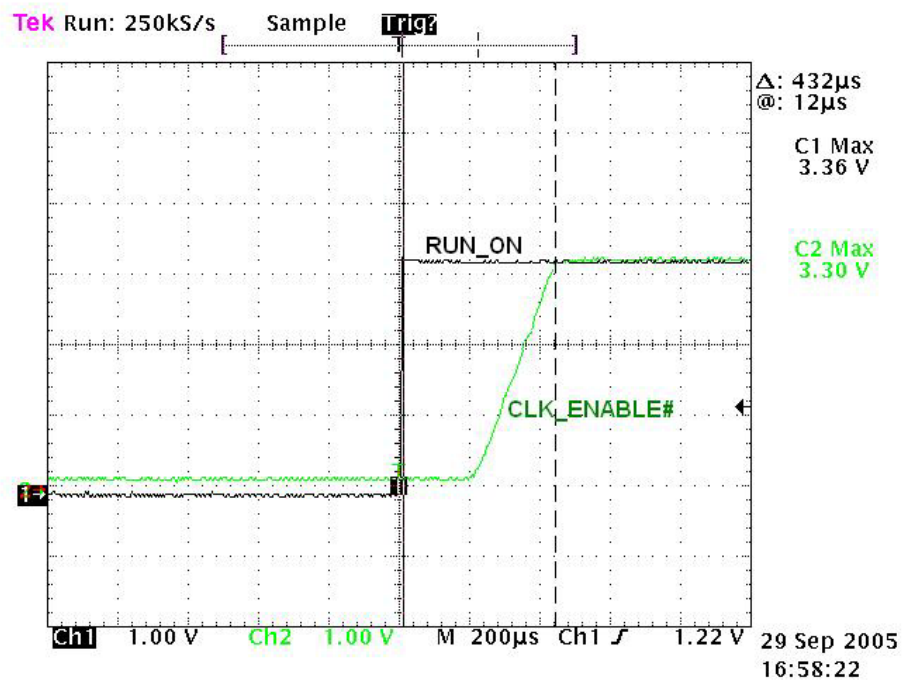


Fig.33 Time of RUN_ON to CLK_ENABLE# -B

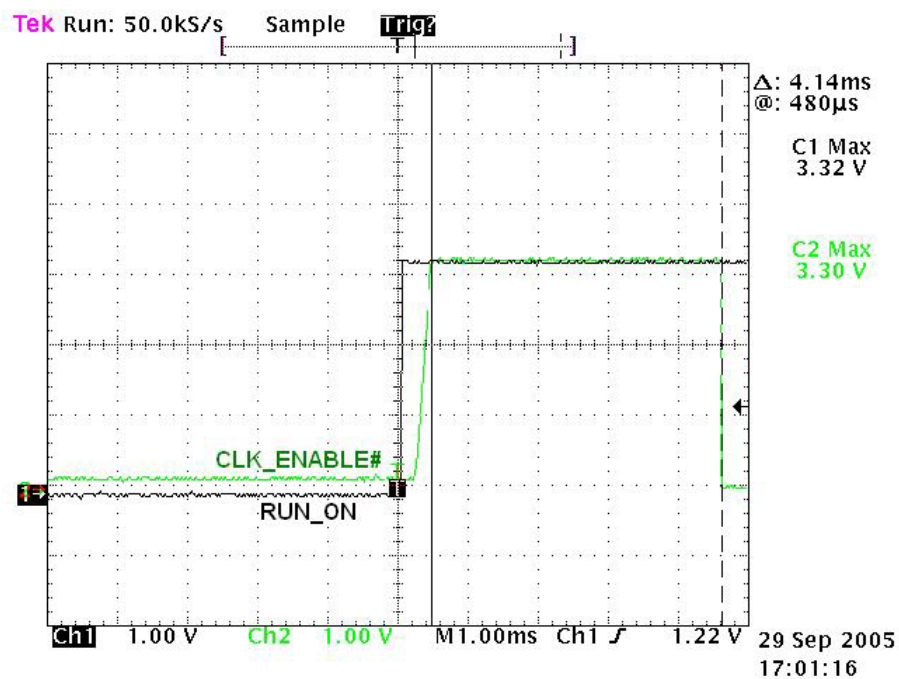


Fig.34 Time of RUN_ON to CLOCKS

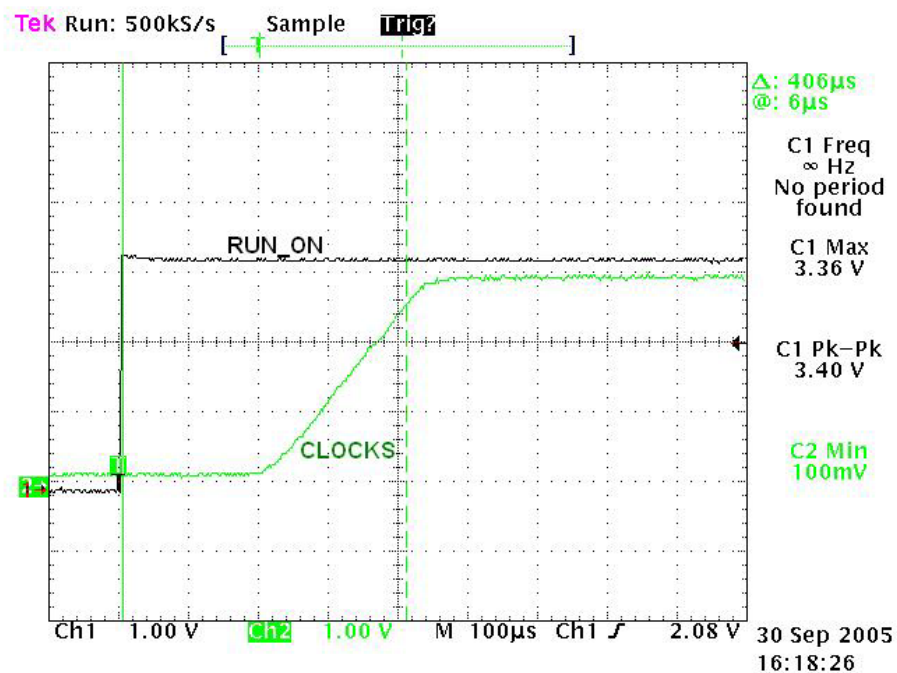


Fig.35 Time of RUN_ON to IMVP_PWRGD

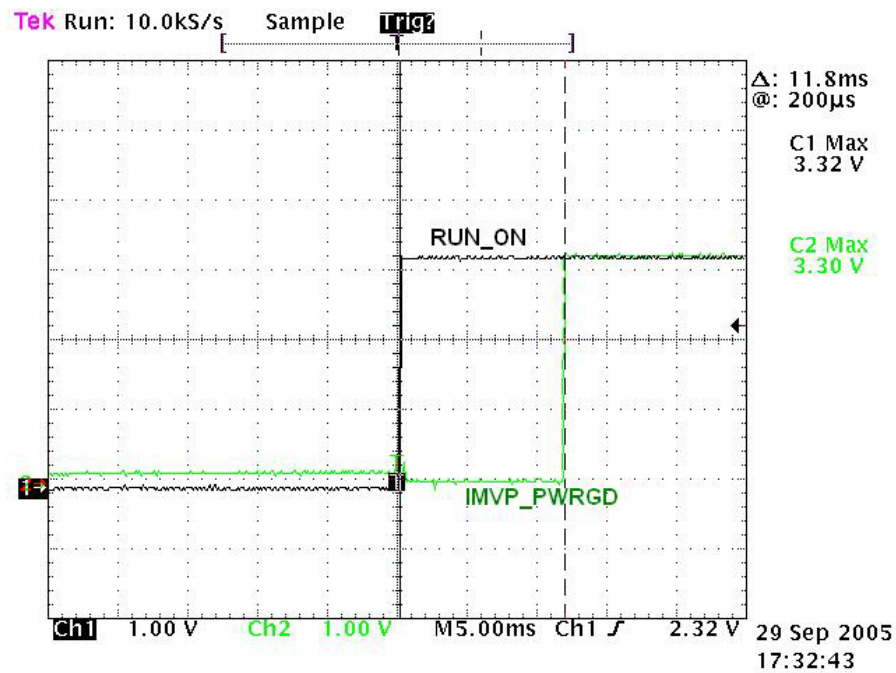


Fig.36 Time of RUN_ON to RESET_OUT

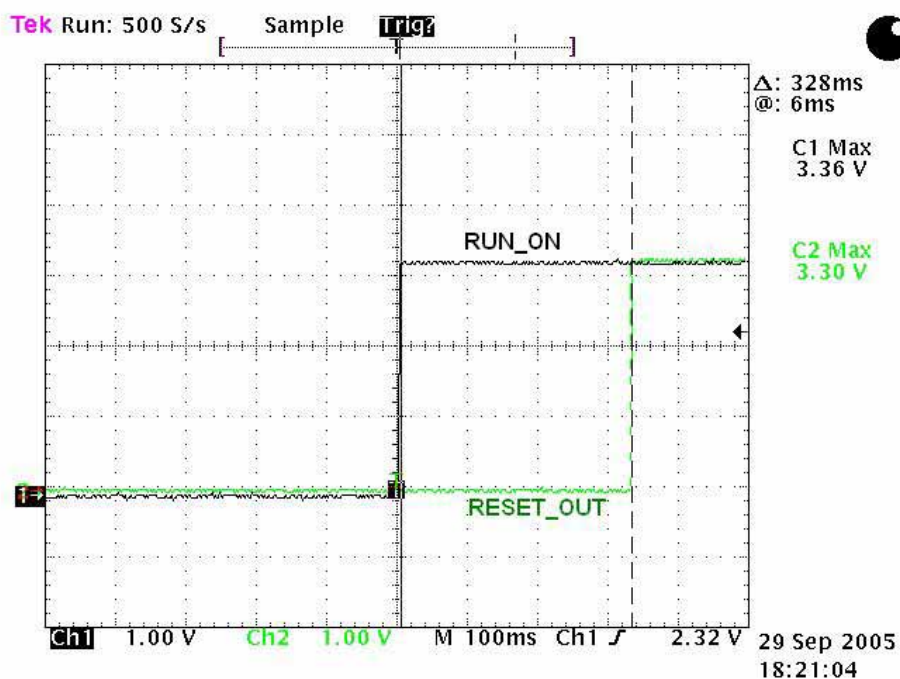


Fig.37 Time of RUN_ON to RESET_OUT

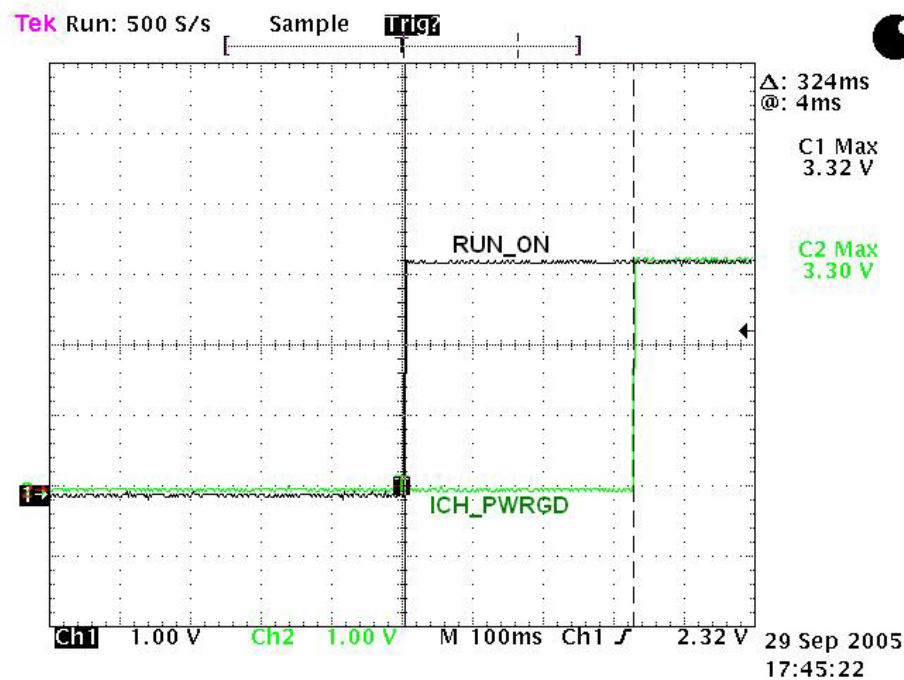


Fig.38 Time of RUN_ON to PLT_RST#

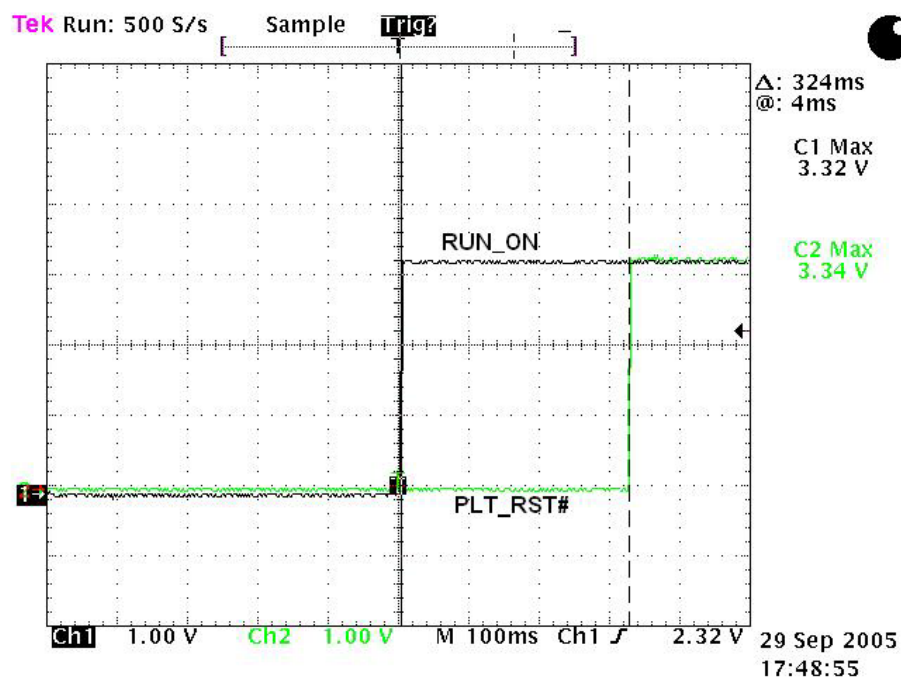




Fig.39 Time of RUN_ON to PCIRST#

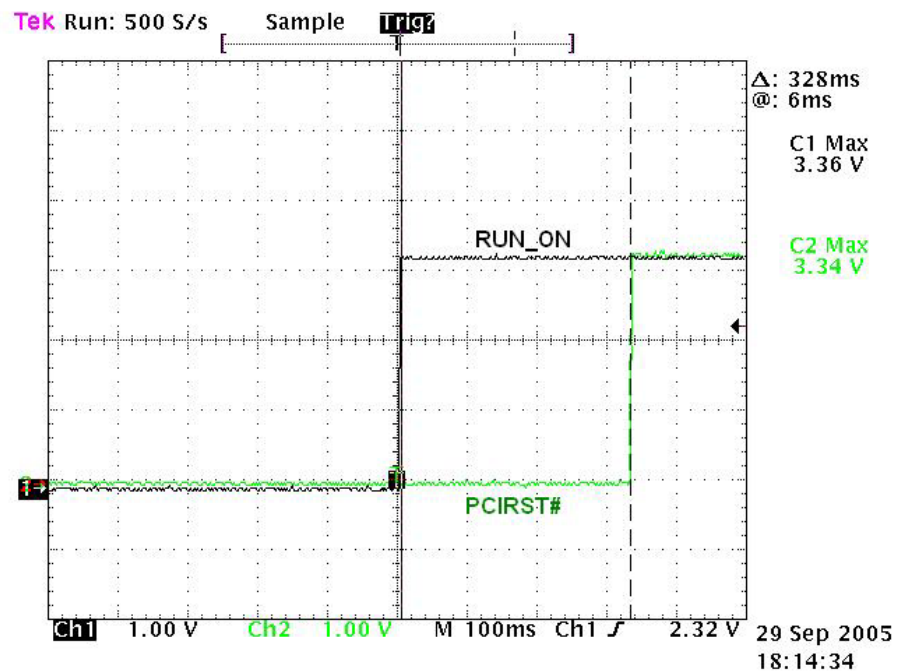


Fig.40 Time of PLT_RST# to H_RESET#

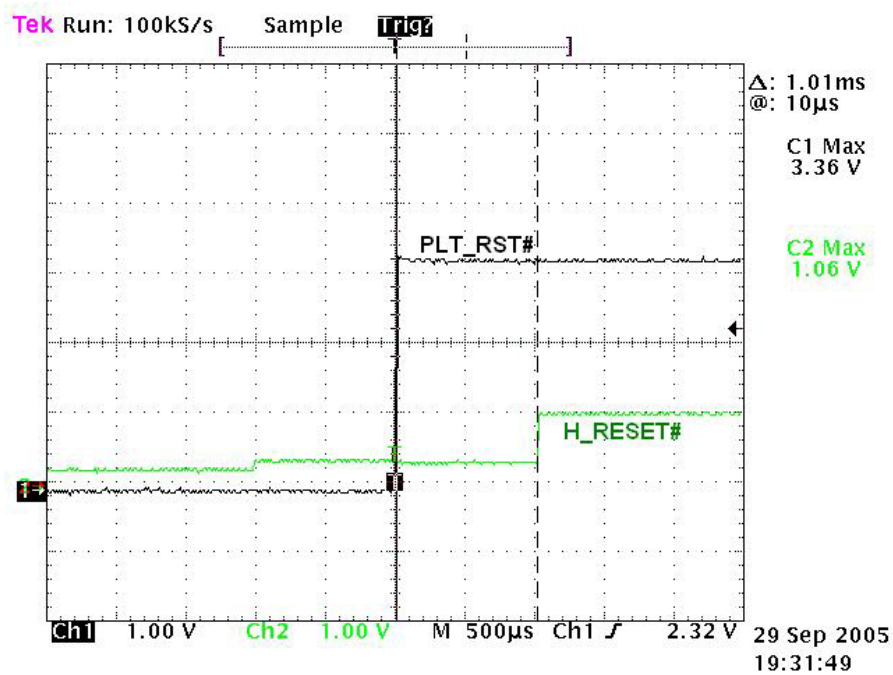




Fig.41 Time of PLT_RST# to ENVDD

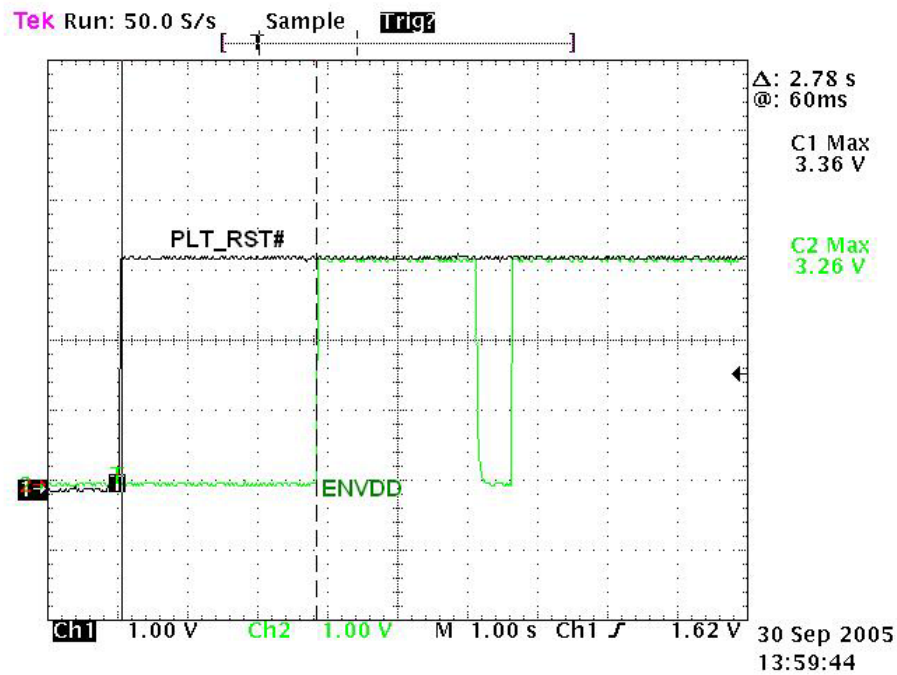


Fig.42 Time of PLT_RST# to LCD_VDD

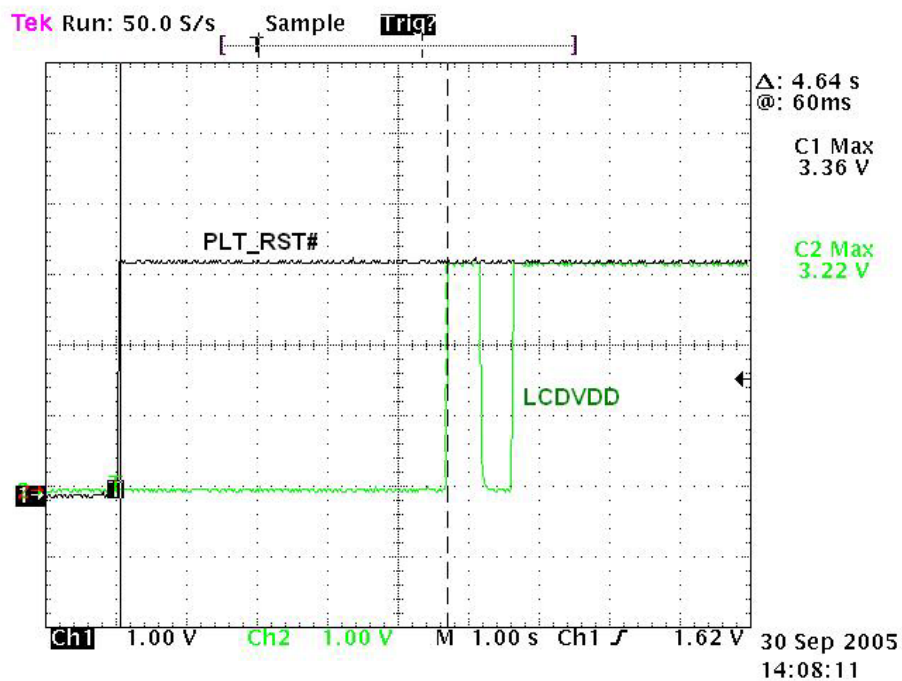
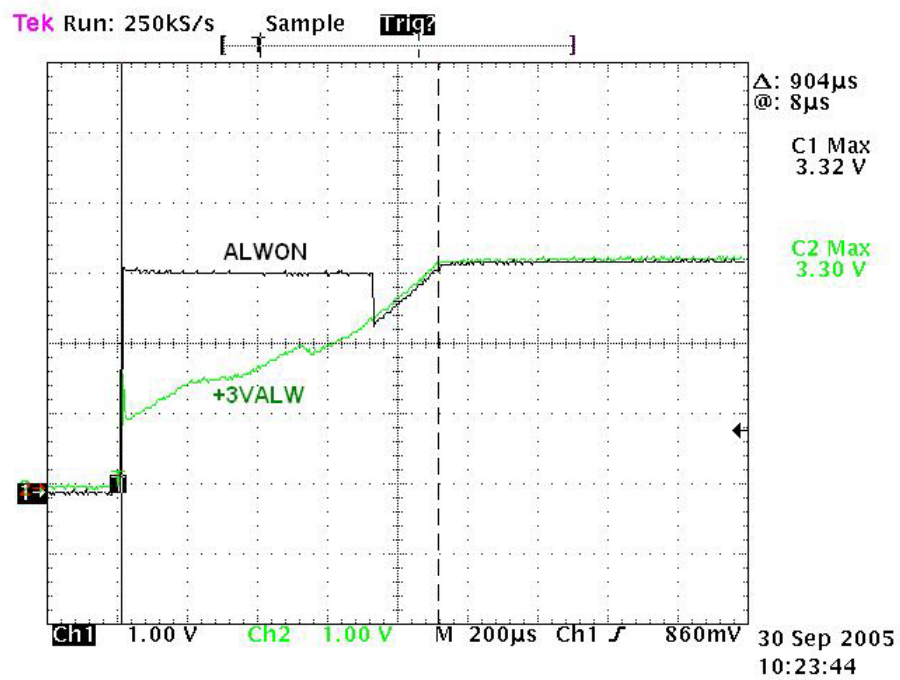




Fig.43 Time of ALWON to +3VALW





Pre-boot System Assessment(PSA) and the DELLDIAG LED Codes :

<i>EVENT</i>	<i>NumLk</i>	<i>CapLk</i>	<i>Scroll</i>	<i>Description</i>
CPU	-	-	ON	The microcontroller is handing control of the system to the Pentium. This code will persist if no processor is installed or if there is no FWH/ROM.
MEMORY	-	FLASH	-	The memory is believed to be good but it's About to be exercised; i.e. when shadowing BIOS and when testing/zeroing all memory.
PCI	-	FLASH	FLASH	Configuring PCI bridges.
VIDEO	-	FLASH	ON	Decompressing video BIOS and executing initialization (video POST).
DASD	-	ON	-	Diskette and hard disk initialization.
USB	-	ON	FLASH	USB controller initialization.
NOMEMORY	-	ON	ON	No SODIMM is installed.
PLANAR	FLASH	-	-	Timer/Gate A20/RTC/mouse-port tests/etc.
SPDERROR	FLASH	-	FLASH	SPD data indicates all SODIMMs are unusable.
CONFIG	FLASH	FLASH	-	Running PCI Option ROMs.
SMI	FLASH	ON	-	Loading SMI handler and executing first SMIs.
PANEL	FLASH	ON	FLASH	Turning on the panel (after video configuration).
DOCK	FLASH	ON	ON	Enabling/configuring the dock.
AUDIO	ON	-	-	AC97 codec detection.
MODEM	ON	-	FLASH	AC97 modem detection.
NIC	ON	-	ON	NIC configuration.
BOOTED	ON	ON	ON	POST has completed; the BIOS is about to jump to the PSA module.

D_Pebble_BIOS_POWER_~1[1].TXT

The current power event codes are:

PWRON	01h	Power on event
(unused)	02h...10h	
PWROFF_FLASH	11h	Power off after BIOS flash upgrade.
PWROFF_AC_REMOVED	12h	Power off due to AC removal with no battery present
PWROFF_BAT_REMOVED	13h	Power off due to battery removal with no AC present
(unused)	14h	
PWROFF_LOBAT	15h	Power off due to low battery condition
PWROFF_PWRB	16h	Power off due to 4-second power button press
(unused)	17h	
PWROFF_FORCE_IMMEDIATE	18h	Power off due to PWROFF_FORCE_xxx when system was not fully on
PWROFF_FORCE_TIMER	19h	Power off because ran off RBATT too long, or timer expired after PWROFF_FORCE_xxx
PWROFF_PWRGOOD_FAIL	1ah	Power off because PWRGOOD went away (run plane voltage dipped)
(unused)	1bh..21h	
PWROFF_FORCE_THERMAL	22h	Power off because CPU temperature stayed above critical level for over 5 seconds
PWROFF_ERR_CODE	23h	Power off because Pentium returned an error from POST
PWROFF_THERMAL_POLL	24h	KBC Polled & temp > critical
(unused)	25h..30h	
SWOFF ACPI	31h	Power off due to ACPI request
SWOFF_APM	32h	Power off due to APM request
SWOFF_BOOT_PASSWORD	33h	Power off due to invalid System Password entry
SWOFF_DISK_PASSWORD	34h	Power off due to invalid Hard Drive Password entry
SWOFF_DOCK	35h	Power off due to connection to unsupported dock
SWOFF_DWIM	36h	Power off due to normal power button press
(unused)	37h	
SWOFF_MODULE	38h	Power off due to inability to identify inserted module
SWOFF_NO_VIDEO	39h	Power off due to no display device available
SWOFF_PNP	3Ah	Power off due to PnP request
(unused)	3Bh..3Eh	
SWOFF_FSMI	3Fh	Power off due to software SMI request
(unused)	40h	
PWRLOG_THERMTRIP	41h	Power off due to THERMTRIP hardware